

SHEET TITLE

01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	LGA775 A
05	LGA775 B
06	LGA775 C
07	LGA775 D
08	GMCH-HOST ,PCIE ,DMI
09	GMCH-DDRII
10	GMCH-VGA ,MISC
11	GMCH-GND
12	GMCH-POWER
13	DDRII CHANNEL A
14	DDRII CHANNEL B
15	DDRII TERMINATION
16	PCIE SLOT X16 ,X1
17	ICH9-PCI ,PCIE ,USB ,DMI
18	ICH9-HOST ,HDA ,LAN ,RTC ,SPI ,LPC ,SATA
19	ICH9-POWER ,GND
20	CKG RTM875T-605
21	PCI SLOT
22	HW MONITOR ,KB/MS ,MECH HOLD
23	FRONT PANEL ,BUZZER
24	FRONT USB
25	FAN CONTROL
26	DISCRETE POWER 1
27	DISCRETE POWER 2

SHEET TITLE

28	SIO ITE8718F
29	COMA/B ,FDD ,LPT
30	JMB368 PATA CONTROLLER
31	PWM NCP5387MNR2G
32	LAN8111C/8101E
33	R USB
34	ATX ,SPI
35	HDA CODEC ALC883
36	HD AUDIO JACK
37	GPIO & RESET
38	
39	
40	
41	
42	

Example Fab Drawing Note

Trace Width (mils)	Differential Spacing (mils)	Impedance	Tolerance
4	NA	50 ohm, single-ended	15%
6.5	NA	40 ohm, single-ended	15%
7.5	NA	37 ohm, single-ended	15%
9.5	NA	32 ohm, single-ended	15%
4	8	95 ohm, differential	20%, reference only
4.5	7.5	90 ohm, differential	20%, reference only

BEARLAKE Impedance Requirements by Interface

Interface	Impedance Required
FSB(ALL)	42 ohm, single-ended
DDR (DQ,DQS,DM,CLK,CLK#)	40 ohm, single-ended
DDR(Control)	37 ohm, single-ended
DDR(Command)	32 ohm, single-ended
PCIE & DMI	95 ohm, differential
VGA	37 ohm, single-ended at (G)MCH breakout, then 50 ohm single-ended to VGA connector.

ICH9 Impedance Requirements by Interface

Interface	Impedance Required
PCI	50 ohm, single-ended
Miscellaneous	50 ohm, single-ended
PCIE & DMI	95 ohm, differential
SATA	95 ohm, differential
USB	90 ohm, differential

4-layer stack-up total thickness=62mils

SIGNAL LAYER	1.9 MILS (Final thickness after plating)
PREPREG 1080HR	2.7 MILS
VCC Layer	1.2 MILS (1 OZ COPPER)
CORE	50 MILS +/-6 mils
GND Layer	1.2 MILS (1 OZ COPPER)
PREPREG 1080HR	2.7 MILS
SIGNAL LAYER	1.9 MILS (Final thickness after plating)

BLOCK DIAGRAM

CLOCK GENERATOR
RTM875T-605

VCC3 = 3.3V

PCI EXPRESS X16

VCC3 = 3.3V
VCC = 5V
+12V=-12V

LAN8111C/8101E

PCI EXPRESS X1

VCC3 = 3.3V
VCC = 5V
+12V=-12V

JMicron JMB368
IDE X1

VCC_2V=2V

USB PORTS 0~7

FUSEVCC=5V

HDA ALC883

INTEL
LGA775

VCCORE = 1.15 - 1.5V
VTT_MCH=1.2V

GMCH
G33 (Bearlake-G)

VTT_GMCH=1.2V
VCC1_25=1.25V
DDR18V=1.8V
VCC3=3.3V

ICH9

VCC1_05_ICH=1.05V
VTT_GMCH=1.2V
VCC1_5_ICH=1.3V
VCC3=3.3V

PCI BUS

PCI SLOT 1

+12 = 12V
-12 = -12V
VCC = 5V
VCC3 = 3V
3VDDUAL = 3V

PCI SLOT 2

+12 = 12V
-12 = -12V
VCC = 5V
VCC3 = 3V
3VDDUAL = 3V

FRONT PANEL /CPU FAN

CHANNEL A
DDRII DIMM X 2

1.8VSTR = 1.8V(MEMORY,SUSPEND POWER)
VTT_DDR = 0.9V

CHANNEL B
DDRII DIMM X 2

1.8VSTR = 1.8V(MEMORY,SUSPEND POWER)
VTT_DDR = 0.9V

SERIAL ATA X4

SPI BIOS

LPC BUS

LPC I/O ITE8718F

I/O PORTS :

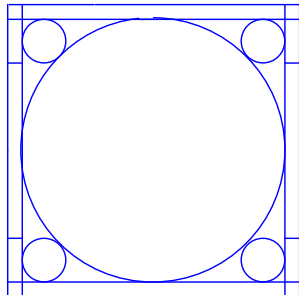
GIGABYTE TECHNOLOGIES , INC.

BOM & PCB MODIFY HISTORY			
File			
Size	Document Number	Rev	
Custom	TG33MK-HP	1.1	
Date	Wednesday, February 15, 2006	Page	2 of 37

Version:1.1

[illegible][illegible]

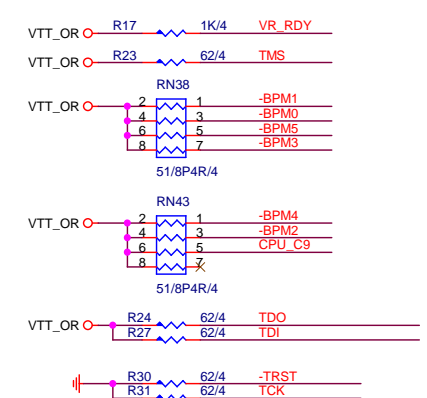
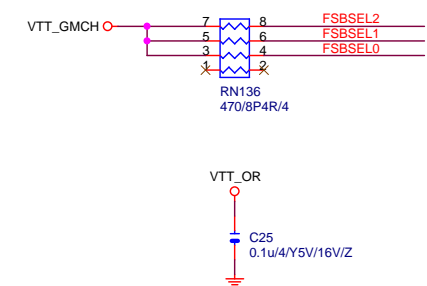
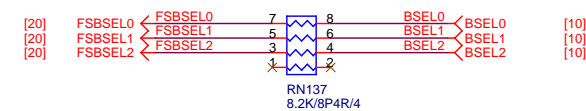
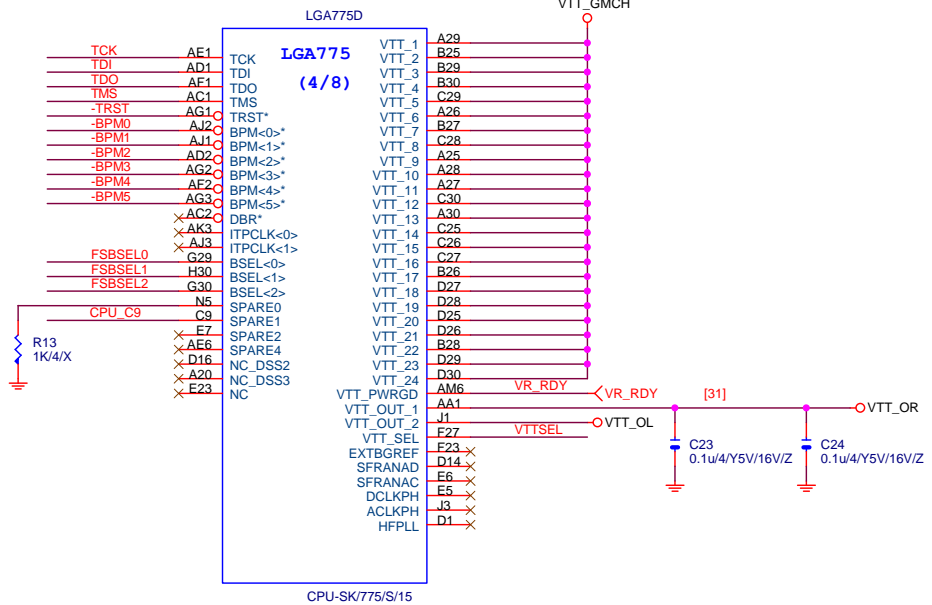
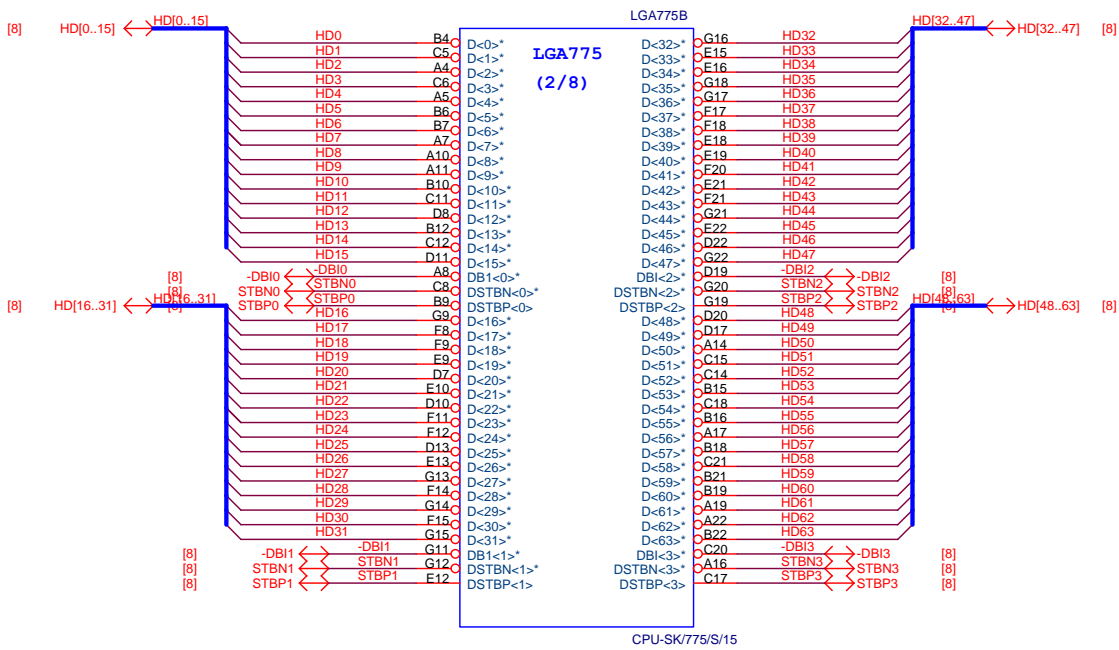
LGA775A



GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

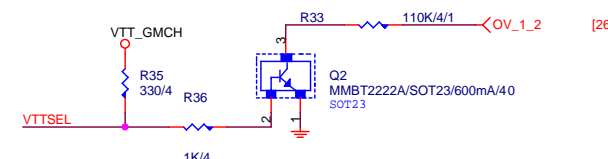
GIGABYTE TECHNOLOGIES, INC.

Title			
P4_LGA775-A			
Size B	Document Number		Rev
	TG33MK-HP		1.1
Date:	Wednesday, February 13, 2008	Sheet	4 of 37



VTTSEL CIRCUIT

VTTSEL	VTT_GMCH
VTTSEL=0	1.2V
VTTSEL=1	1.1V



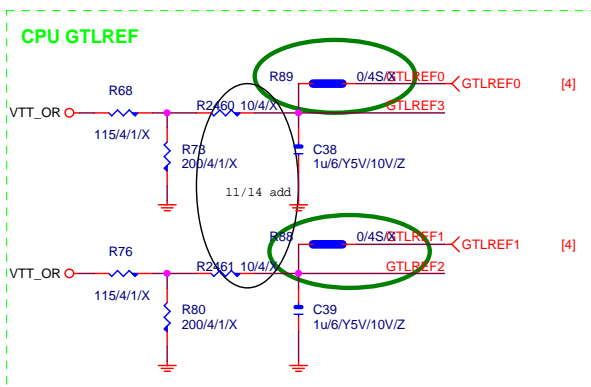
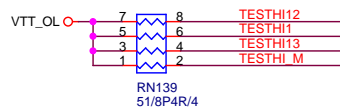
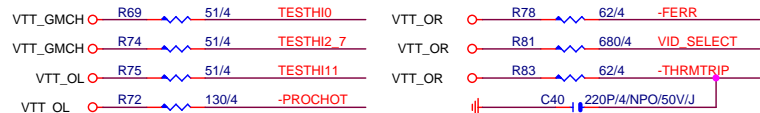
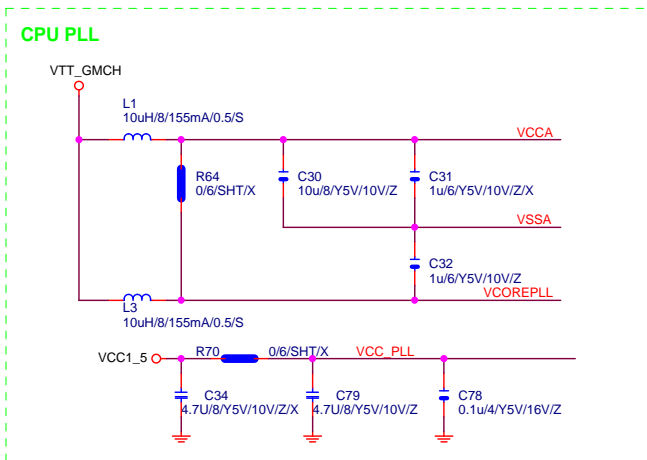
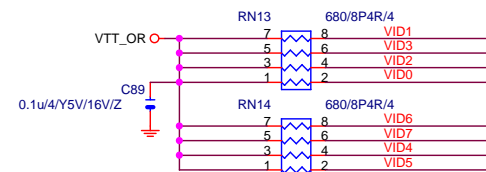
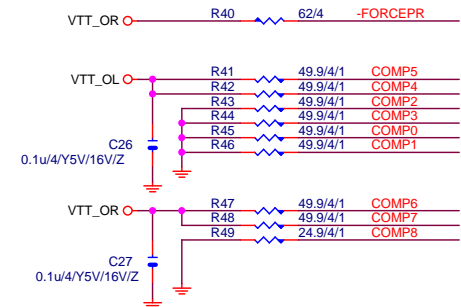
FSA	FSB	FSC	
FSBSEL0	FSBSEL1	FSBSEL2	Clock
1	0	1	100MHz
1	0	0	133MHz
1	1	0	166MHz
0	1	0	200MHz
0	0	0	266MHz
0	0	1	333MHz

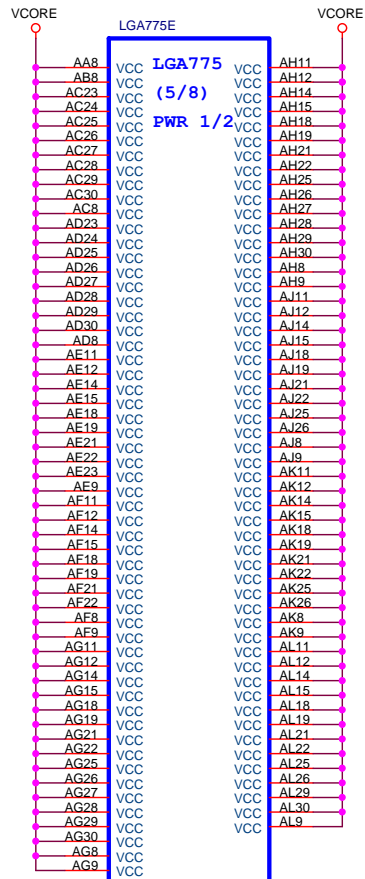
GIGABYTE TECHNOLOGIES, INC.

Title: P4_LGA775-C

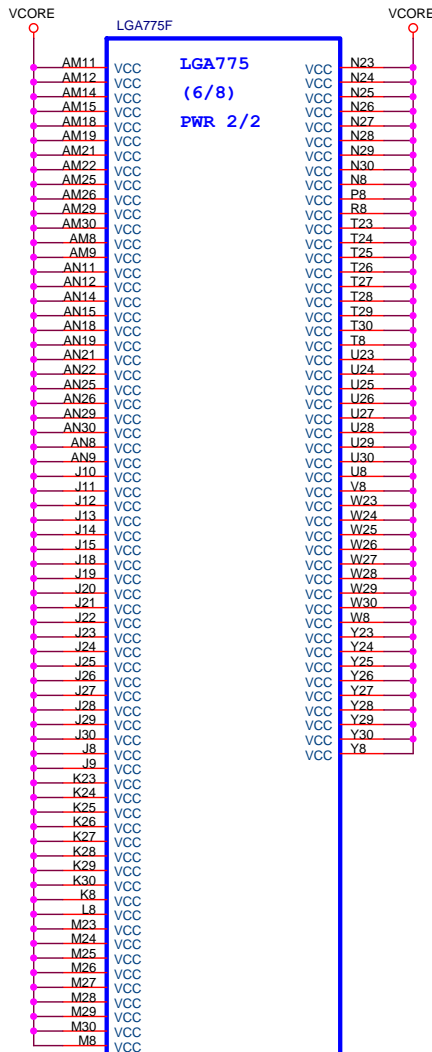
Size B: Document Number: TG33MK-HP Rev 1.1

Date: Wednesday, February 13, 2008 Sheet 5 of 37

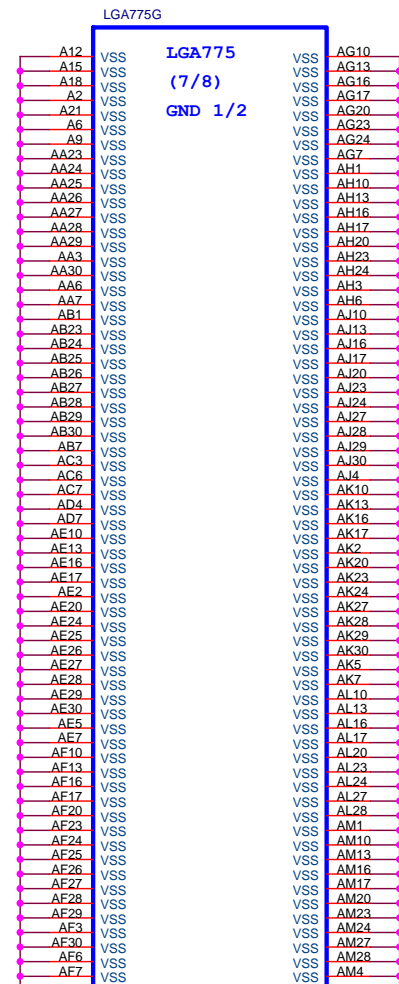




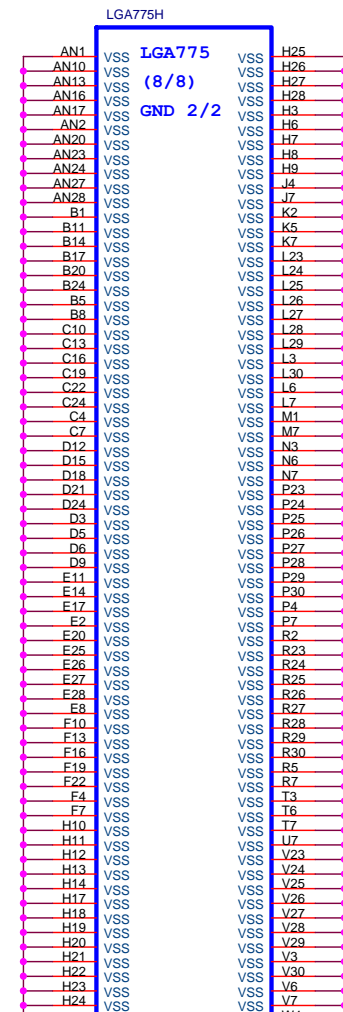
CPU-SK/775/S/15



CPU-SK/775/S/15



CPU-SK/775/S/15



CPU-SK/775/S/15

GIGABYTE TEHCHNOLOGIES, INC.

Title				P4_LGA775-D			
Size B	Document Number			TG33MK-HP			Rev 1.
Date:	Wednesday, February 13, 2008			Sheet	7	of	37

MODT_A0_31 ↔ MODT_A0[0..3] [13..15]

U2C

MAAA0 BB30
MAAA1 AY25
MAAA2 BA23
MAAA3 BB23
MAAA4 AY23
MAAA5 BA22
MAAA6 BB21
MAAA7 AW21
MAAA8 BA21
MAAA9 BB31
MAAA10 BB31
MAAA11 AY21
MAAA12 BC20
MAAA13 AY38
MAAA14 BA19

[13..15] -SWEA ↔ -SCASA BA33
[13..15] -SCASA ↔ -SRASA AW35
[13..15] -SRASA ↔ -SBAA0 BA31
[13..15] SBAA0 ↔ SBAA1 AY31
[13..15] SBAA1 ↔ SBAA2 AY20

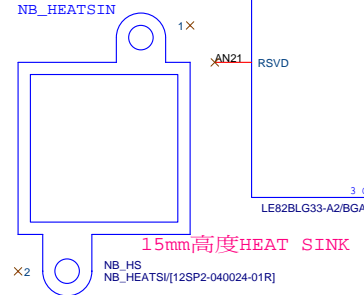
[13..15] -CSA0 ↔ -CSA1 BA34
[13..15] -CSA1 ↔ -CSA2 AY35
[13..15] -CSA2 ↔ -CSA3 BB33
[13..15] -CSA3 ↔ -CCKE0 AY19

[13..15] CKEA0 ↔ CKEA1 AW18
[13..15] CKEA1 ↔ CKEA2 BB19
[13..15] CKEA2 ↔ CKEA3 BA18
[13..15] CKEA3 ↔ MODT_A0 BB35

MODT_A1 BA38
MODT_A2 BA35
MODT_A3 BA39

[13] DCLKA0 ↔ DCLKA0 AR31
[13] DCLKA0 ↔ DCLKA0 AU31
[13] DCLKA1 ↔ DCLKA1 AN27
[13] DCLKA1 ↔ DCLKA1 AY33
[13] DCLKA2 ↔ DCLKA2 AW33
[13] DCLKA2 ↔ DCLKA2 AP29
[13] DCLKA3 ↔ DCLKA3 AP31
[13] DCLKA4 ↔ DCLKA4 AM26
[13] DCLKA4 ↔ DCLKA4 AM27
[13] DCLKA5 ↔ DCLKA5 AT33
[13] DCLKA5 ↔ DCLKA5 AU33

DDR_A



DDR_A_DQS_0 AP2 DQSA0
DDR_A_DQS_0 AP3 DQSA0
DDR_A_DM_0 AN2 DMA0
DDR_A_DM_0 AM1 MDA0
DDR_A_DM_0 AN3 MDA2
DDR_A_DM_0 AR3 MDA3
DDR_A_DM_0 AL3 MDA4
DDR_A_DM_0 AM2 MDA5
DDR_A_DM_0 AR4 MDA7
DDR_A_DM_0 AW2 DQSA1
DDR_A_DM_0 AW1 DQSA1
DDR_A_DM_0 AW3 DMA1

DDR_A_DM_0 AV4 MDA8
DDR_A_DM_0 AV3 MDA9
DDR_A_DM_0 BA4 MDA10
DDR_A_DM_0 AU2 MDA12
DDR_A_DM_0 AU1 MDA13
DDR_A_DM_0 AY2 MDA14
DDR_A_DM_0 AY3 MDA15

DDR_A_DM_0 AY7 DQSA2
DDR_A_DM_0 BA6 DQSA2
DDR_A_DM_0 BB6 DMA2
DDR_A_DM_0 BB5 MDA16
DDR_A_DM_0 AY6 MDA17
DDR_A_DM_0 BA9 MDA18
DDR_A_DM_0 BB9 MDA19
DDR_A_DM_0 BA5 MDA20
DDR_A_DM_0 BB4 MDA21
DDR_A_DM_0 BC7 MDA22
DDR_A_DM_0 AY9 MDA23

DDR_A_DM_0 AT20 DQSA3
DDR_A_DM_0 AU18 DQSA3
DDR_A_DM_0 AN18 DMA3
DDR_A_DM_0 AT18 MDA24
DDR_A_DM_0 AR18 MDA25
DDR_A_DM_0 AU21 MDA26
DDR_A_DM_0 AT21 MDA27
DDR_A_DM_0 AP17 MDA28
DDR_A_DM_0 AN17 MDA29
DDR_A_DM_0 AP20 MDA30
DDR_A_DM_0 AV20 MDA31

DDR_A_DM_0 AR41 DQSA4
DDR_A_DM_0 AR40 DQSA4
DDR_A_DM_0 AU43 DMA4
DDR_A_DM_0 AV42 MDA32
DDR_A_DM_0 AU40 MDA33
DDR_A_DM_0 AP42 MDA34
DDR_A_DM_0 AN39 MDA35
DDR_A_DM_0 AV40 MDA36
DDR_A_DM_0 AV41 MDA37
DDR_A_DM_0 AR42 MDA38
DDR_A_DM_0 AP41 MDA39

DDR_A_DM_0 AL41 DQSA5
DDR_A_DM_0 AL40 DQSA5
DDR_A_DM_0 AM43 DMA5
DDR_A_DM_0 AN41 MDA40
DDR_A_DM_0 AM39 MDA41
DDR_A_DM_0 AK42 MDA42
DDR_A_DM_0 AK41 MDA43
DDR_A_DM_0 AN40 MDA44
DDR_A_DM_0 AN42 MDA45
DDR_A_DM_0 AL42 MDA46
DDR_A_DM_0 AL39 MDA47

DDR_A_DM_0 AG42 DQSA6
DDR_A_DM_0 AG41 DQSA6
DDR_A_DM_0 AG40 DMA6
DDR_A_DM_0 AJ40 MDA48
DDR_A_DM_0 AH43 MDA49
DDR_A_DM_0 AF39 MDA50
DDR_A_DM_0 AE40 MDA51
DDR_A_DM_0 AJ42 MDA52
DDR_A_DM_0 AJ41 MDA53
DDR_A_DM_0 AF41 MDA54
DDR_A_DM_0 AF42 MDA55

DDR_A_DM_0 AC42 DQSA7
DDR_A_DM_0 AC41 DQSA7
DDR_A_DM_0 AC40 DMA7
DDR_A_DM_0 AD40 MDA56
DDR_A_DM_0 AD43 MDA57
DDR_A_DM_0 AB41 MDA58
DDR_A_DM_0 AA40 MDA59
DDR_A_DM_0 AE42 MDA60
DDR_A_DM_0 AE41 MDA61
DDR_A_DM_0 AC39 MDA62
DDR_A_DM_0 AB42 MDA63

DDR_A_DM_0 AL41 DQSA5
DDR_A_DM_0 AL40 DQSA5
DDR_A_DM_0 AM43 DMA5
DDR_A_DM_0 AN41 MDA40
DDR_A_DM_0 AM39 MDA41
DDR_A_DM_0 AK42 MDA42
DDR_A_DM_0 AK41 MDA43
DDR_A_DM_0 AN40 MDA44
DDR_A_DM_0 AN42 MDA45
DDR_A_DM_0 AL42 MDA46
DDR_A_DM_0 AL39 MDA47

DDR_A_DM_0 AG42 DQSA6
DDR_A_DM_0 AG41 DQSA6
DDR_A_DM_0 AG40 DMA6
DDR_A_DM_0 AJ40 MDA48
DDR_A_DM_0 AH43 MDA49
DDR_A_DM_0 AF39 MDA50
DDR_A_DM_0 AE40 MDA51
DDR_A_DM_0 AJ42 MDA52
DDR_A_DM_0 AJ41 MDA53
DDR_A_DM_0 AF41 MDA54
DDR_A_DM_0 AF42 MDA55

DDR_A_DM_0 AC42 DQSA7
DDR_A_DM_0 AC41 DQSA7
DDR_A_DM_0 AC40 DMA7
DDR_A_DM_0 AD40 MDA56
DDR_A_DM_0 AD43 MDA57
DDR_A_DM_0 AB41 MDA58
DDR_A_DM_0 AA40 MDA59
DDR_A_DM_0 AE42 MDA60
DDR_A_DM_0 AE41 MDA61
DDR_A_DM_0 AC39 MDA62
DDR_A_DM_0 AB42 MDA63

DDR_A_DM_0 AL41 DQSA5
DDR_A_DM_0 AL40 DQSA5
DDR_A_DM_0 AM43 DMA5
DDR_A_DM_0 AN41 MDA40
DDR_A_DM_0 AM39 MDA41
DDR_A_DM_0 AK42 MDA42
DDR_A_DM_0 AK41 MDA43
DDR_A_DM_0 AN40 MDA44
DDR_A_DM_0 AN42 MDA45
DDR_A_DM_0 AL42 MDA46
DDR_A_DM_0 AL39 MDA47

DDR_A_DM_0 AG42 DQSA6
DDR_A_DM_0 AG41 DQSA6
DDR_A_DM_0 AG40 DMA6
DDR_A_DM_0 AJ40 MDA48
DDR_A_DM_0 AH43 MDA49
DDR_A_DM_0 AF39 MDA50
DDR_A_DM_0 AE40 MDA51
DDR_A_DM_0 AJ42 MDA52
DDR_A_DM_0 AJ41 MDA53
DDR_A_DM_0 AF41 MDA54
DDR_A_DM_0 AF42 MDA55

DDR_A_DM_0 AC42 DQSA7
DDR_A_DM_0 AC41 DQSA7
DDR_A_DM_0 AC40 DMA7
DDR_A_DM_0 AD40 MDA56
DDR_A_DM_0 AD43 MDA57
DDR_A_DM_0 AB41 MDA58
DDR_A_DM_0 AA40 MDA59
DDR_A_DM_0 AE42 MDA60
DDR_A_DM_0 AE41 MDA61
DDR_A_DM_0 AC39 MDA62
DDR_A_DM_0 AB42 MDA63

MAAB0 AW15
MAAB1 BB15
MAAB2 BA15
MAAB3 AY15
MAAB4 BA14
MAAB5 BB14
MAAB6 AW12
MAAB7 BB12
MAAB8 BA13
MAAB9 AY13
MAAB10 BA17
MAAB11 AY12
MAAB12 BA11
MAAB13 AY27
MAAB14 BB11

[14..15] -SWEA ↔ -SCASB BB25
[14..15] -SCASB ↔ -SRASB AW26
[14..15] -SRASB ↔ SBAB0 BB17
[14..15] SBAB0 ↔ SBAB1 AY17
[14..15] SBAB1 ↔ SBAB2 AY11

[14..15] -CSB0 ↔ -CSB1 BA25
[14..15] -CSB1 ↔ -CSB2 BA29
[14..15] -CSB2 ↔ -CSB3 BA30
[14..15] CKEB0 ↔ CKEB1 AW11
[14..15] CKEB1 ↔ CKEB2 BC12
[14..15] CKEB2 ↔ CKEB3 BB10
[14..15] CKEB3 ↔ MODT_B0 BB27

MODT_B1 AW29
MODT_B2 BA27
MODT_B3 AY29

[14] DCLKB0 ↔ DCLKB0 AW31
[14] DCLKB0 ↔ DCLKB0 AV31
[14] DCLKB1 ↔ DCLKB1 AU27
[14] DCLKB1 ↔ DCLKB1 AT27
[14] DCLKB2 ↔ DCLKB2 AV32
[14] DCLKB2 ↔ DCLKB2 AR29
[14] DCLKB3 ↔ DCLKB3 AU29
[14] DCLKB3 ↔ DCLKB3 AV29
[14] DCLKB4 ↔ DCLKB4 AW27
[14] DCLKB4 ↔ DCLKB5 AN33
[14] DCLKB5 ↔ DCLKB5 AP32

TP15 ↔ BA2
TP16 ↔ AN32
TP17 ↔ AM31
TP18 ↔ AG32
TP19 ↔ AF32
TP20 ↔ AP21
TP21 ↔ AA39
TP22 ↔ BA2

U2D

DDR_B_MA_0
DDR_B_MA_1
DDR_B_MA_2
DDR_B_MA_3
DDR_B_MA_4
DDR_B_MA_5
DDR_B_MA_6
DDR_B_MA_7
DDR_B_MA_8
DDR_B_MA_9
DDR_B_MA_10
DDR_B_MA_11
DDR_B_MA_12
DDR_B_MA_13
DDR_B_MA_14

DDR_B_WEB
DDR_B_CASB
DDR_B_RASB
DDR_B_BS_0
DDR_B_BS_1
DDR_B_BS_2

DDR_B_CSB_0
DDR_B_CSB_1
DDR_B_CSB_2
DDR_B_CSB_3
DDR_B_CKE_0
DDR_B_CKE_1
DDR_B_CKE_2
DDR_B_CKE_3

DDR_B_ODT_0
DDR_B_ODT_1
DDR_B_ODT_2
DDR_B_ODT_3

DDR_B_CK_0
DDR_B_CK_1
DDR_B_CK_2
DDR_B_CK_3
DDR_B_CK_4
DDR_B_CK_5

DDR_B_CK_0
DDR_B_CK_1
DDR_B_CK_2
DDR_B_CK_3
DDR_B_CK_4
DDR_B_CK_5

DDR_B_DQS_0
DDR_B_DQS_1
DDR_B_DQS_2
DDR_B_DQS_3
DDR_B_DQS_4
DDR_B_DQS_5

DDR_B_DQS_0
DDR_B_DQS_1
DDR_B_DQS_2
DDR_B_DQS_3
DDR_B_DQS_4
DDR_B_DQS_5

DDR_B_DQS_0
DDR_B_DQS_1
DDR_B_DQS_2
DDR_B_DQS_3
DDR_B_DQS_4
DDR_B_DQS_5

DDR_B_DQS_0
DDR_B_DQS_1
DDR_B_DQS_2
DDR_B_DQS_3
DDR_B_DQS_4
DDR_B_DQS_5

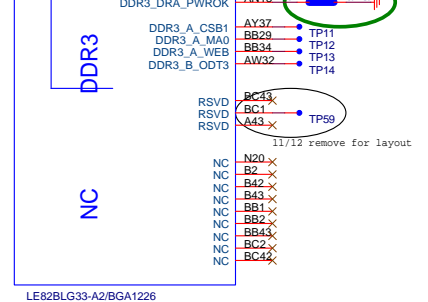
DDR_B_DQS_0
DDR_B_DQS_1
DDR_B_DQS_2
DDR_B_DQS_3
DDR_B_DQS_4
DDR_B_DQS_5

DDR_B_DQS_0
DDR_B_DQS_1
DDR_B_DQS_2
DDR_B_DQS_3
DDR_B_DQS_4
DDR_B_DQS_5

DDR_B_DQS_0
DDR_B_DQS_1
DDR_B_DQS_2
DDR_B_DQS_3
DDR_B_DQS_4
DDR_B_DQS_5

AV6 DQSB0
AU6 DQSB0
AR7 DMB0
AN7 DMB0
AN8 DMB1
AW5 DMB2
AW7 DMB3
AN5 DMB4
AN6 DMB5
AN9 DMB6
AU7 DMB7
AR12 DQSB1
AP12 DQSB1
AW9 DMB1
AT11 DMB8
AU11 DMB9
AP13 DMB10
AR13 DMB11
AU9 DMB12
AU12 DMB13
AU12 DMB15
AP15 DQSB2
AR15 DQSB2
AW13 DMB2
AU15 DMB16
AU13 DMB17
AU17 DMB18
AT17 DMB19
AU13 DMB20
AU13 DMB21
AU15 DMB22
AU17 DMB23
AT24 DQSB3
AU26 DQSB3
AP23 DMB3
AV24 DMB24
AT23 DMB25
AT26 DMB26
AP26 DMB27
AU23 DMB28
AR24 DMB29
AN26 DMB31
AW39 DQSB4
AU39 DQSB4
AU37 DMB4
AW37 DMB32
AV36 DMB33
AN36 DMB34
AN37 DMB35
AU35 DMB36
AR35 DMB37
AN35 DMB38
AR37 DMB39
AL35 DQSB5
AL34 DQSB5
AM37 DMB5
AM35 DMB40
AM38 DMB41
AJ34 DMB42
AL38 DMB43
AR39 DMB44
AM34 DMB45
AL37 DMB46
AL32 DMB47
AG35 DQSB6
AG36 DQSB6
AG39 DMB6
AG38 DMB48
AJ38 DMB49
AF35 DMB50
AF33 DMB51
AJ37 DMB52
AJ35 DMB53
AG33 DMB54
AF34 DMB55
AC36 DQSB7
AC37 DQSB7
AD38 DMB7
AD36 DMB56
AC33 DMB57
AA34 DMB58
AA36 DMB59
AD34 DMB60
AF38 DMB61
AC34 DMB62
AA33 DMB63

U2J

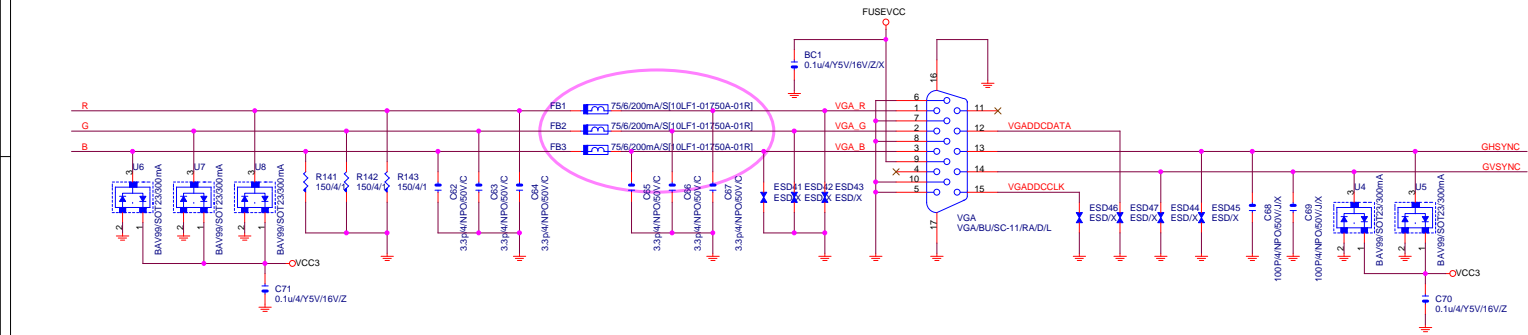


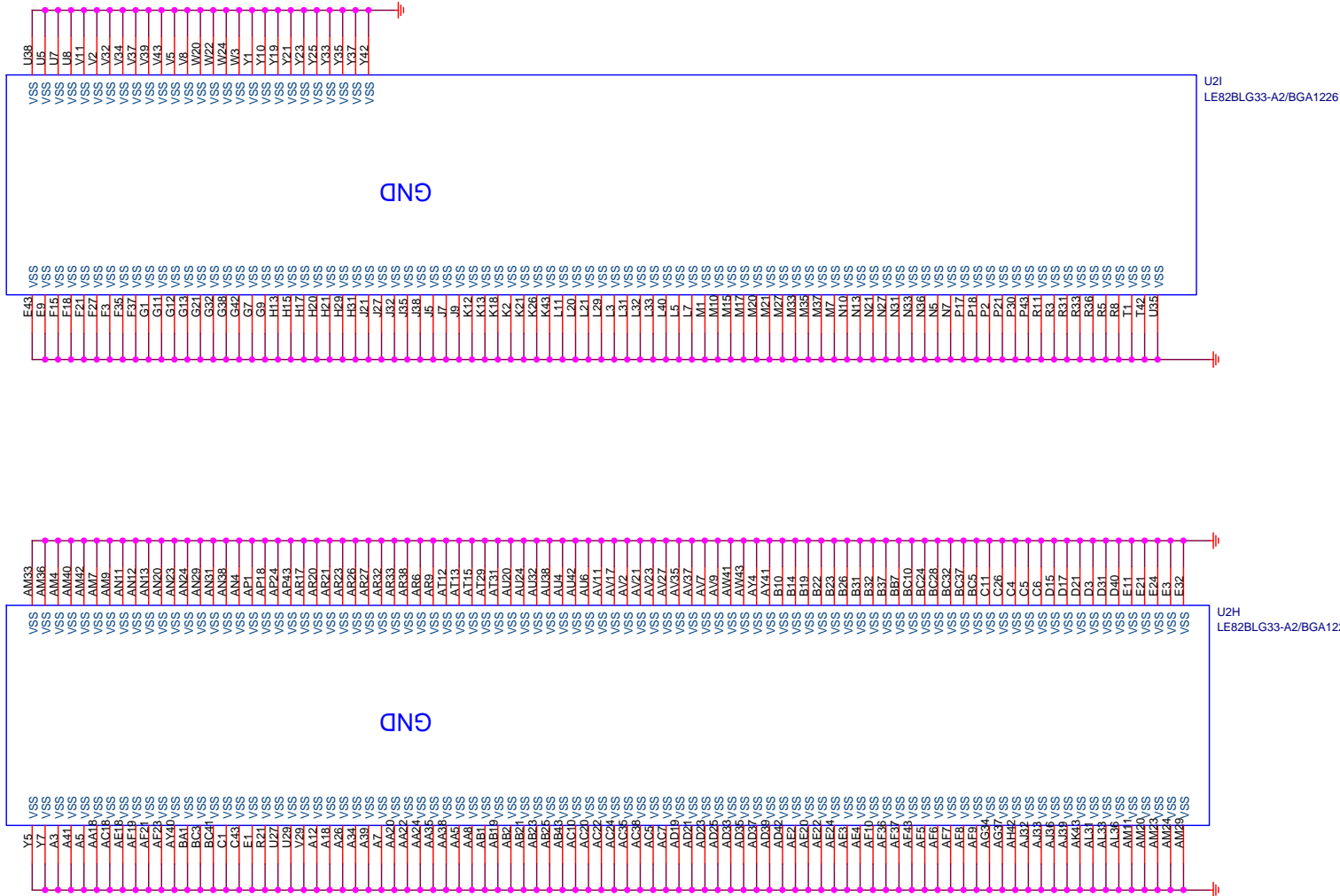
LE82BLG33-A2/BGA1226

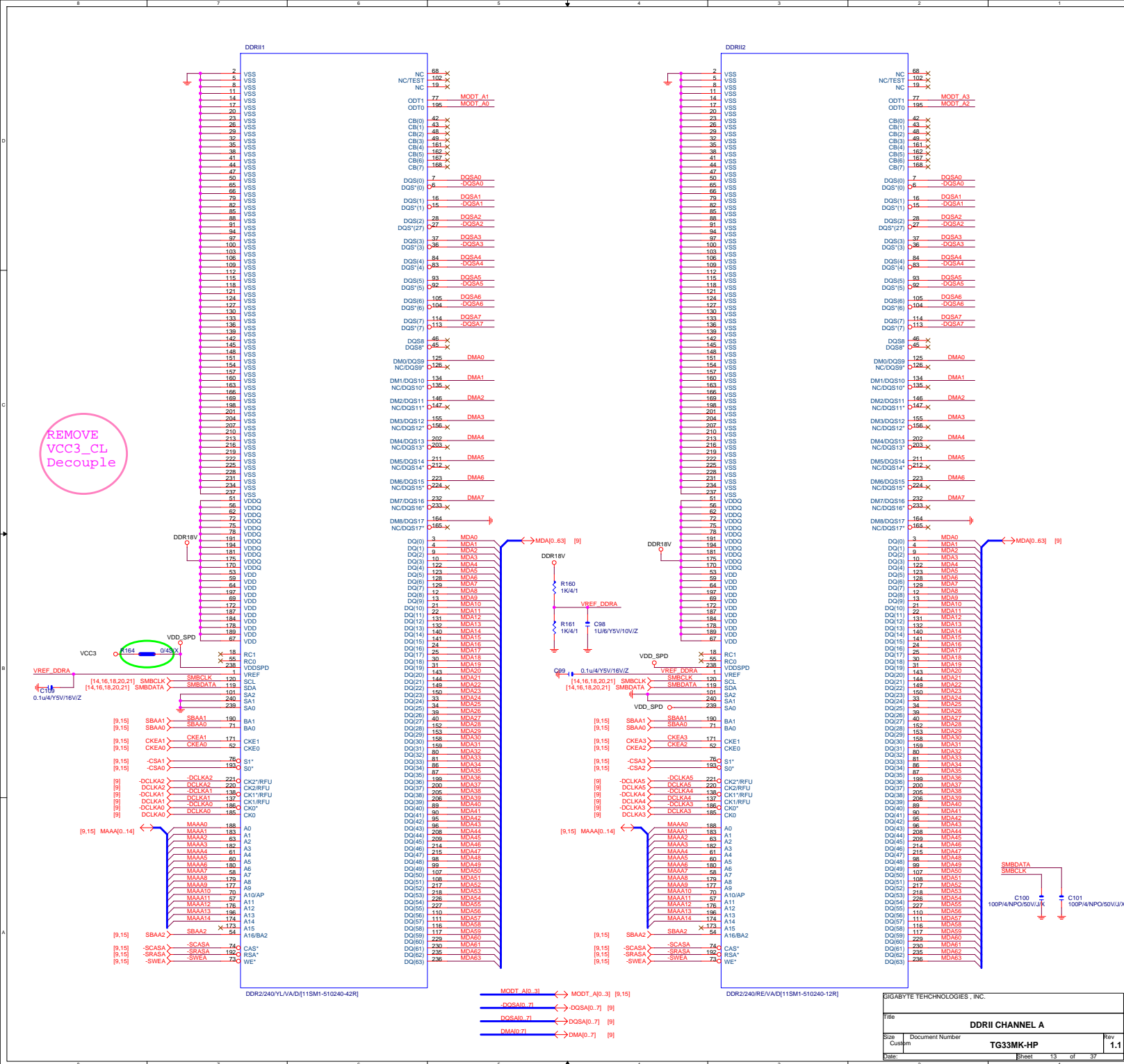
MODT_B0_31 ↔ MODT_B0[0..3] [14..15]

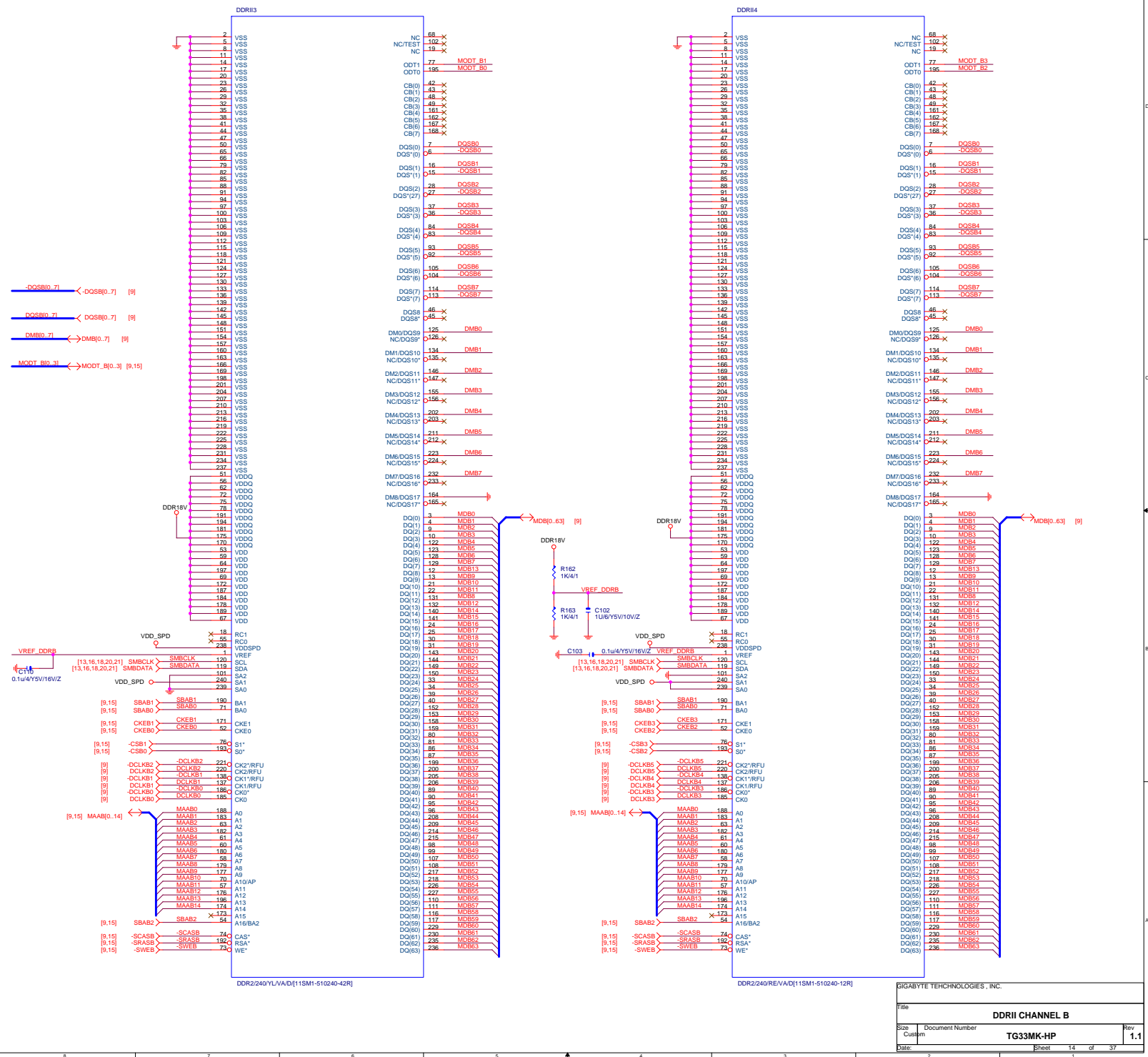
[14] -DQSB[0..7] ↔ -DQSB[0..7]
[14..15] MAAB[0..14] ↔ MAAB[0..14]
[14] DMB[0..7] ↔ DMB[0..7]
[14] MDB[0..63] ↔ MDB[0..63]
[14] DQSB[0..7] ↔ DQSB[0..7]
[13..15] MAAA[0..14] ↔ MAAA[0..14]
[13] DMA[0..7] ↔ DMA[0..7]
[13] MDA[0..63] ↔ MDA[0..63]
[13] DQSA[0..7] ↔ DQSA[0..7]
[13] -DQSA[0..7] ↔ -DQSA[0..7]

GIGABYTE TECHNOLOGIES, INC.		
Title		
GMCH-DDRII		
Size	Document Number	Rev
Custom	TG33MK-HP	1.1
Date:	Wednesday, February 13, 2008	Sheet 9 of 37



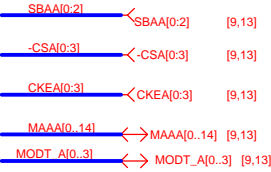
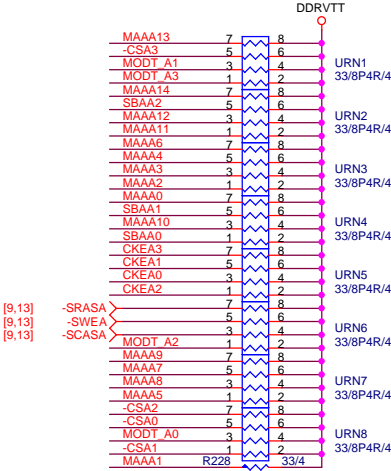
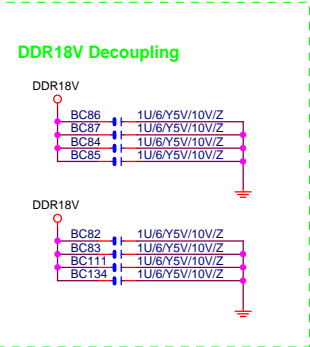
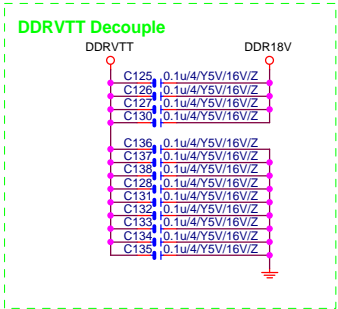
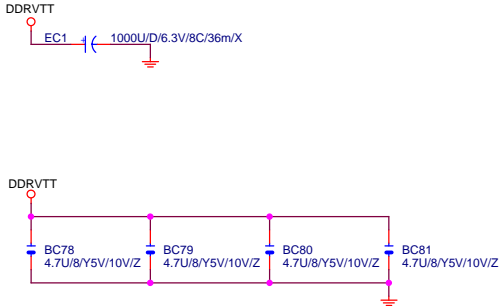




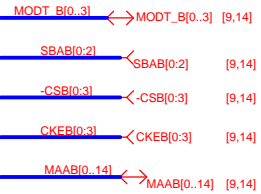
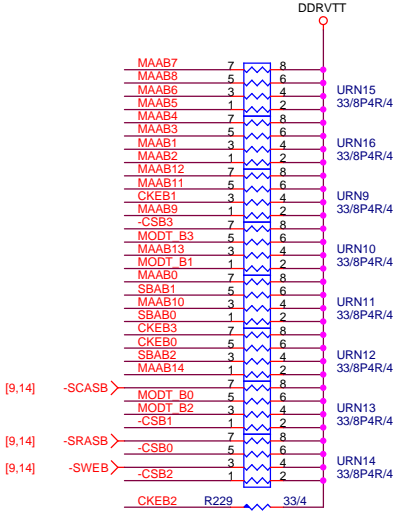
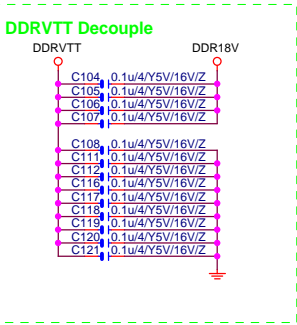


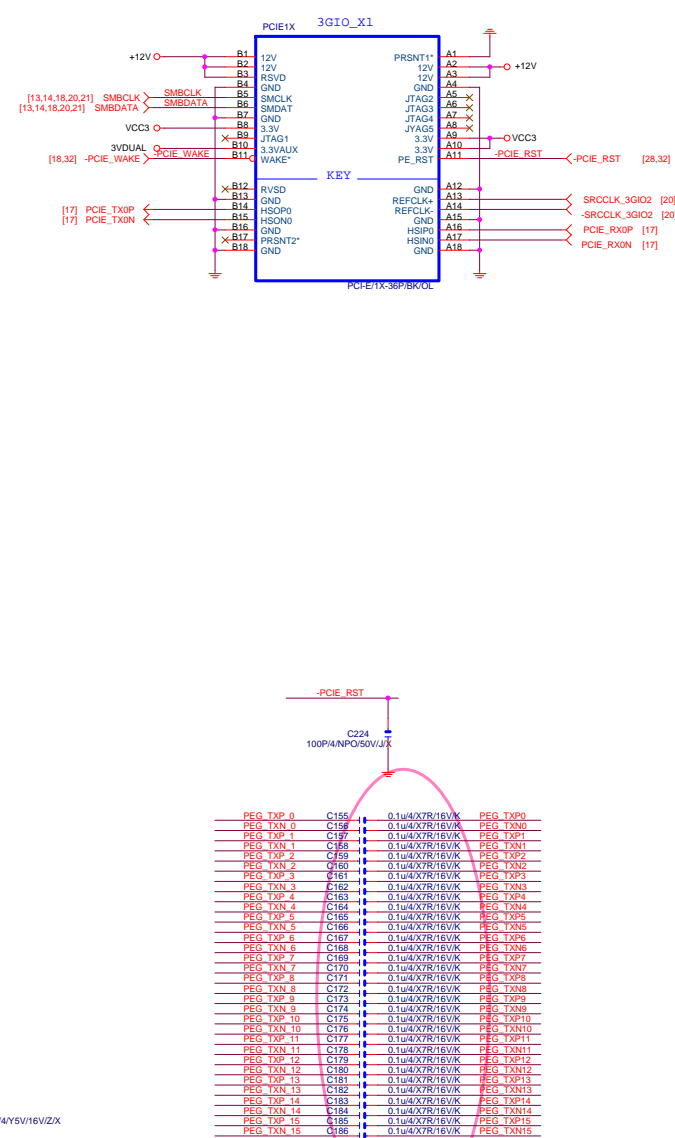
SILIGABYTE TECHNOLOGIES, INC.	
Title	DDRII CHANNEL B
Size	Document Number
Custom	TG33MK-HP
Date	Rev 1.1
Sheet 14 of 37	

DDR TERMINATION
CHANNEL A

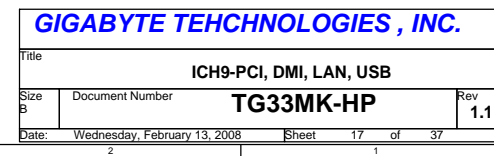


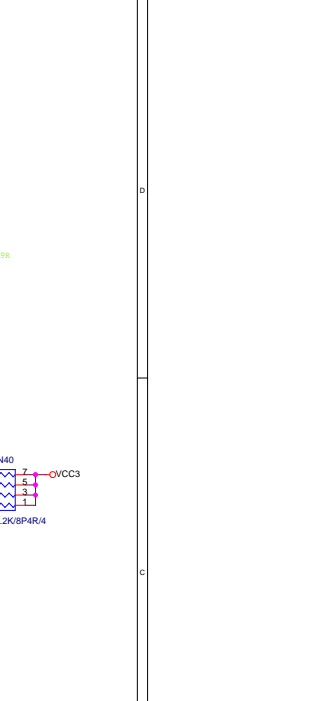
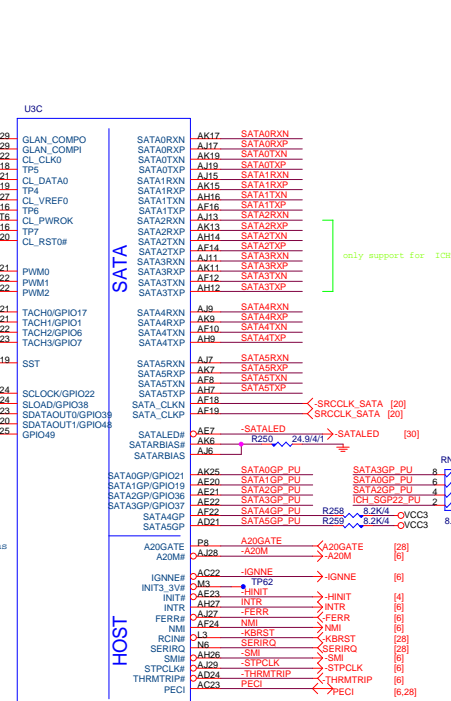
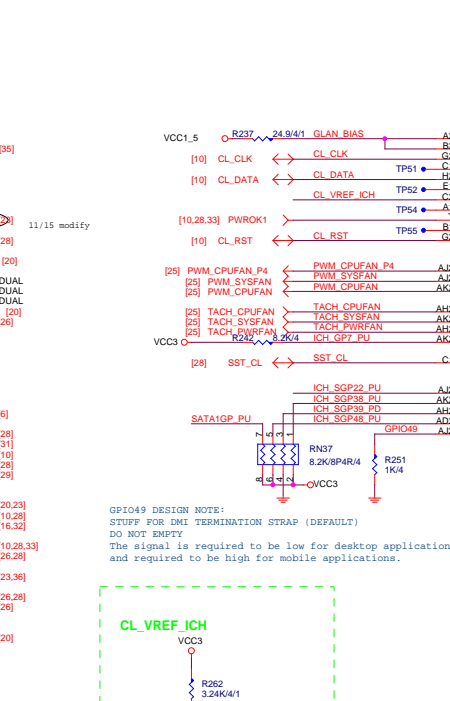
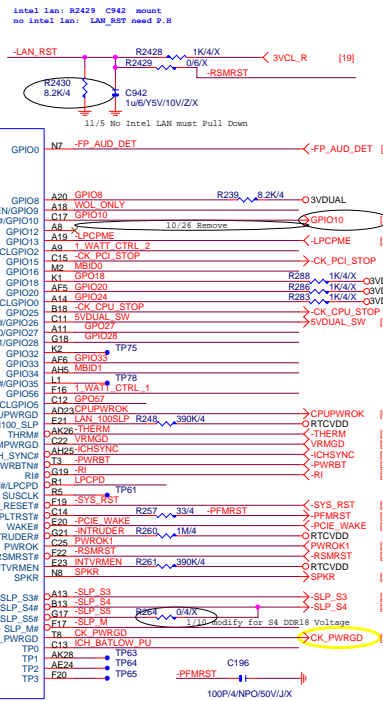
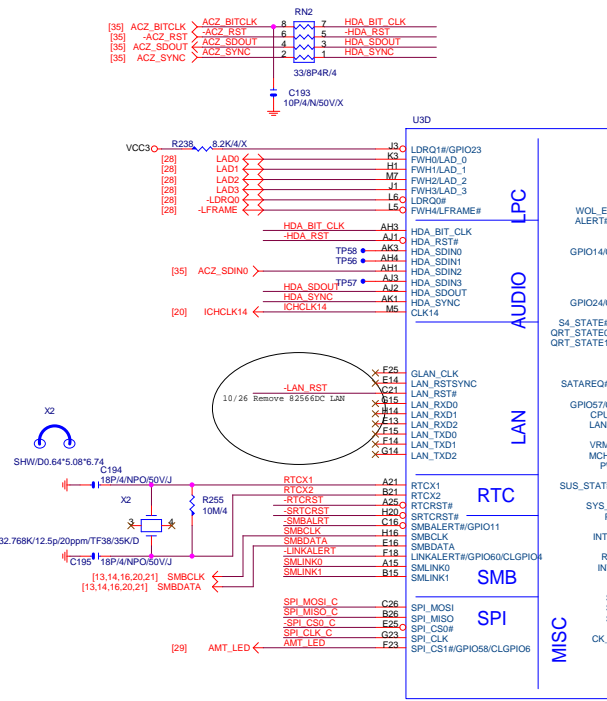
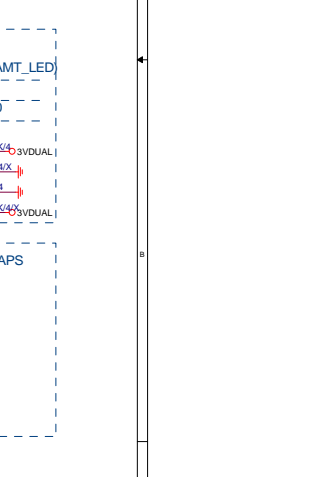
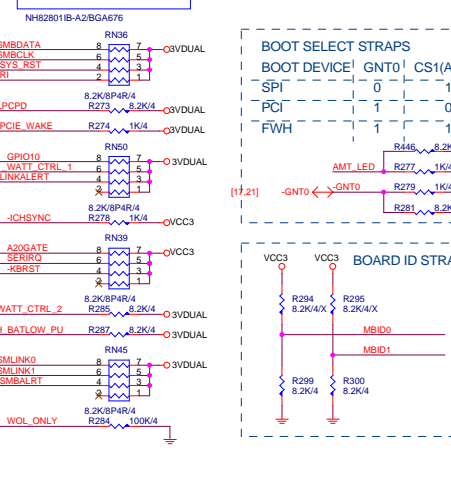
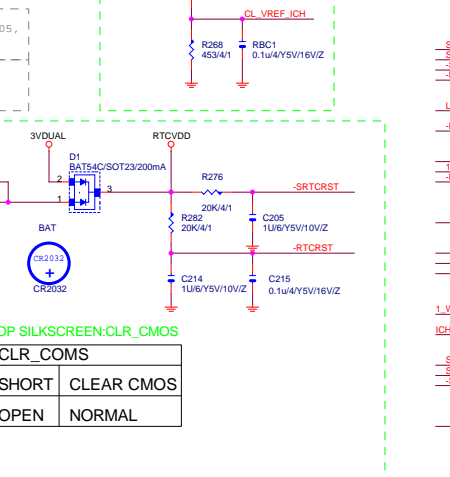
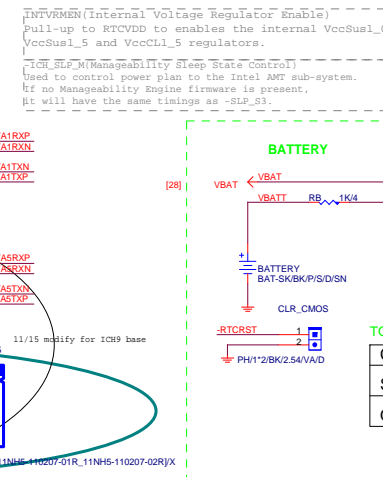
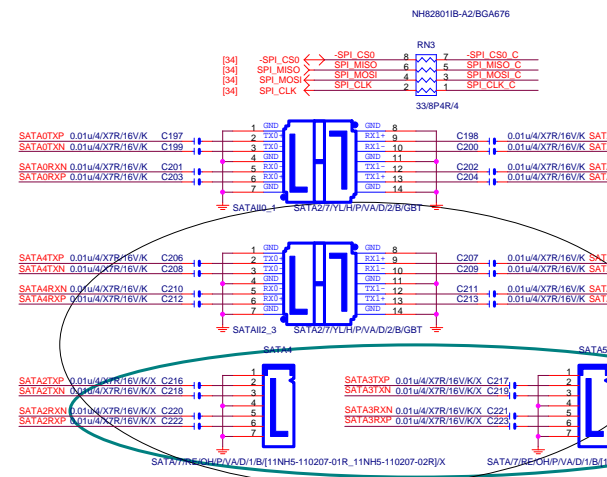
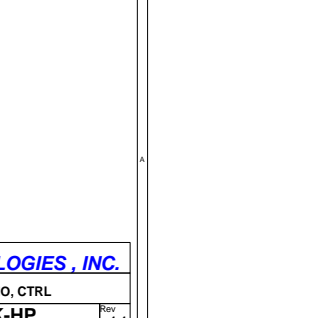
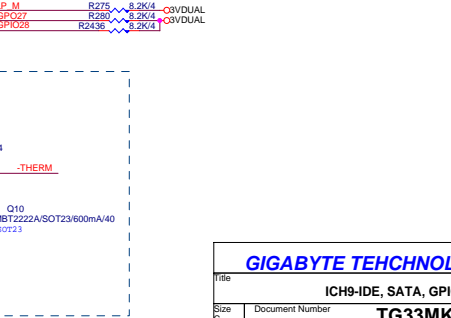
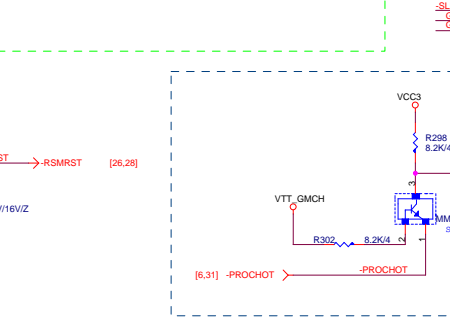
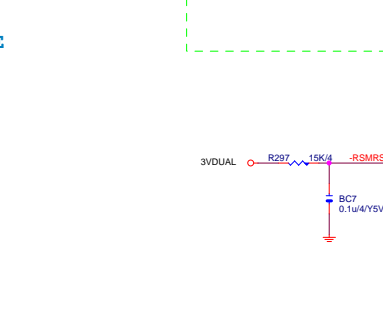
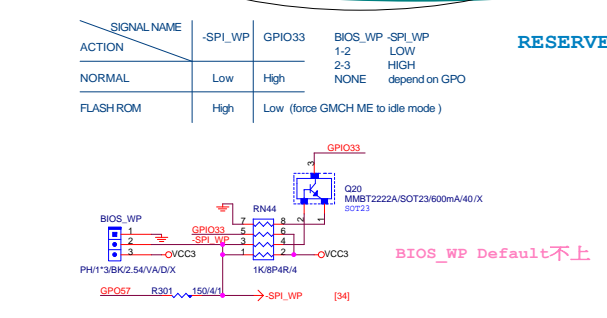
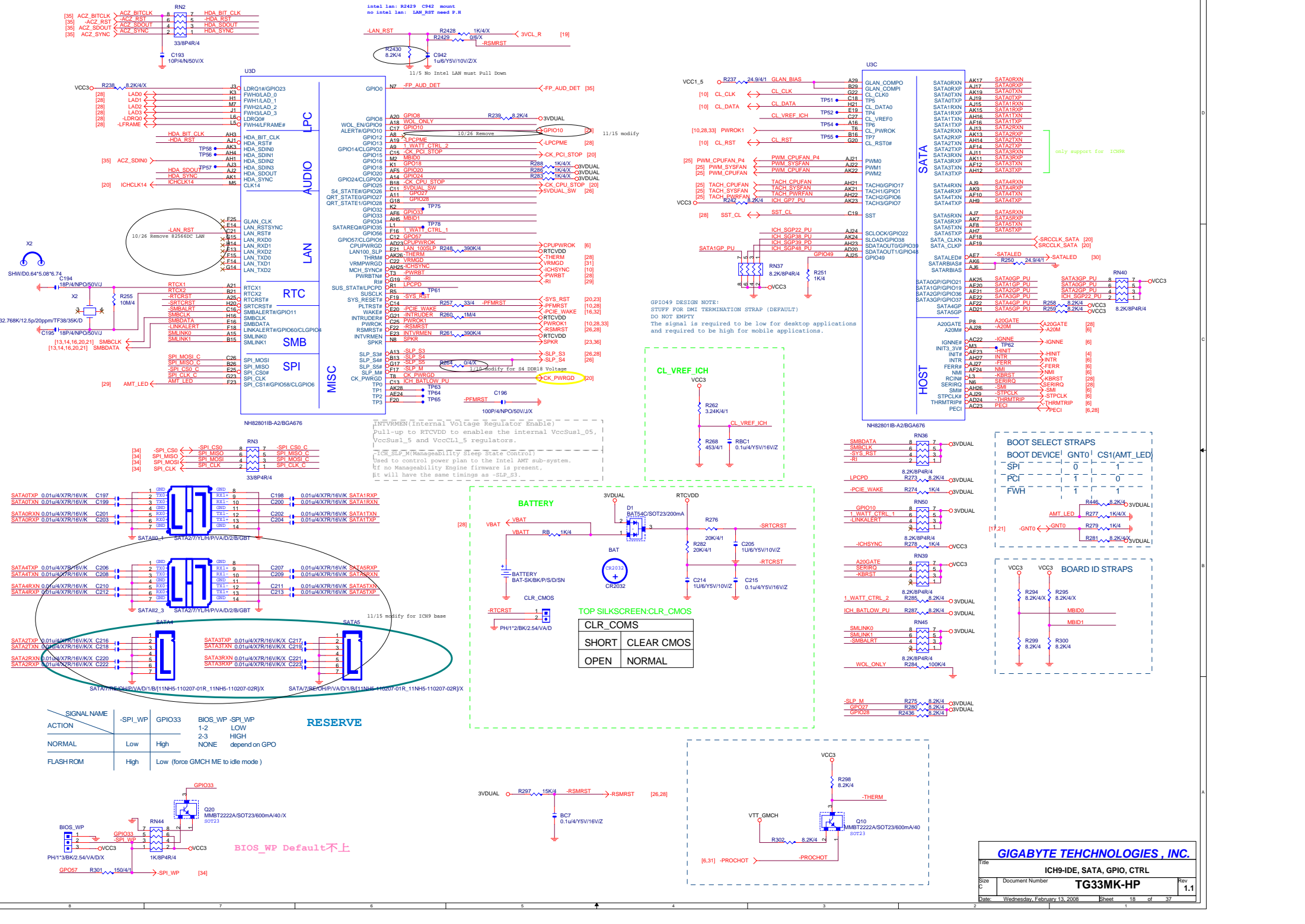
CHANNEL B





PEP_XP_0	C155	0.1u4/x7r76vK	PEP_XP70
PEP_XP_N	C156	0.1u4/x7r76vK	PEP_XP80
PEP_XP_1	C157	0.1u4/x7r76vK	PEP_XP90
PEP_XP_N1	C158	0.1u4/x7r76vK	PEP_XP_N1
PEP_XP_2	C159	0.1u4/x7r76vK	PEP_XP_X
PEP_XP_3	C160	0.1u4/x7r76vK	PEP_XP_Y
PEP_XP_3	C161	0.1u4/x7r76vK	PEP_XP_Z
PEP_XP_4	C162	0.1u4/x7r76vK	PEP_XP_A
PEP_XP_4	C163	0.1u4/x7r76vK	PEP_XP_B
PEP_XP_N4	C164	0.1u4/x7r76vK	PEP_XP_M4
PEP_XP_5	C165	0.1u4/x7r76vK	PEP_XP_C
PEP_XP_5	C166	0.1u4/x7r76vK	PEP_XP_D
PEP_XP_6	C167	0.1u4/x7r76vK	PEP_XP_E
PEP_XP_6	C168	0.1u4/x7r76vK	PEP_XP_F
PEP_XP_7	C169	0.1u4/x7r76vK	PEP_XP_G
PEP_XP_7	C170	0.1u4/x7r76vK	PEP_XP_H
PEP_XP_8	C171	0.1u4/x7r76vK	PEP_XP_I
PEP_XP_N8	C172	0.1u4/x7r76vK	PEP_XP_N8
PEP_XP_9	C173	0.1u4/x7r76vK	PEP_XP_J
PEP_XP_N9	C174	0.1u4/x7r76vK	PEP_XP_N9
PEP_XP_10	C175	0.1u4/x7r76vK	PEP_XP_K
PEP_XP_N10	C176	0.1u4/x7r76vK	PEP_XP_M10
PEP_XP_11	C177	0.1u4/x7r76vK	PEP_XP_L
PEP_XP_11	C178	0.1u4/x7r76vK	PEP_XP_M
PEP_XP_12	C179	0.1u4/x7r76vK	PEP_XP12
PEP_XP_12	C180	0.1u4/x7r76vK	PEP_XP13
PEP_XP_13	C181	0.1u4/x7r76vK	PEP_XP13
PEP_XP_13	C182	0.1u4/x7r76vK	PEP_XP13
PEP_XP_N14	C183	0.1u4/x7r76vK	PEP_XP14
PEP_XP_N14	C184	0.1u4/x7r76vK	PEP_XP14
PEP_XP_N15	C185	0.1u4/x7r76vK	PEP_XP15
PEP_XP_N15	C186	0.1u4/x7r76vK	PEP_XP15



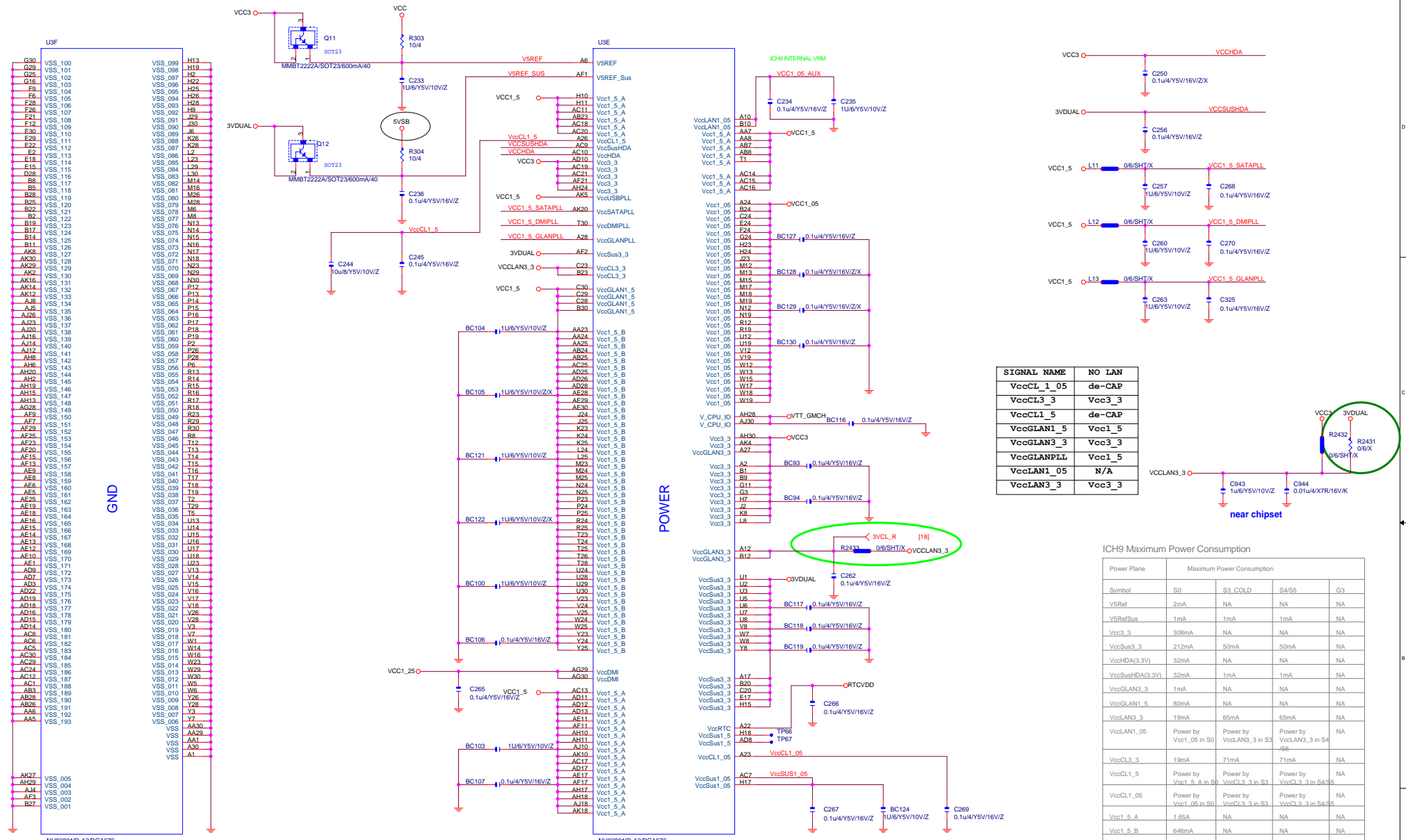


GIGABYTE TECHNOLOGIES, INC.

ICH9-IDE, SATA, GPIO, CTRL

TG33MK-HP

Date: Wednesday, February 13, 2008 Sheet 18 of 37



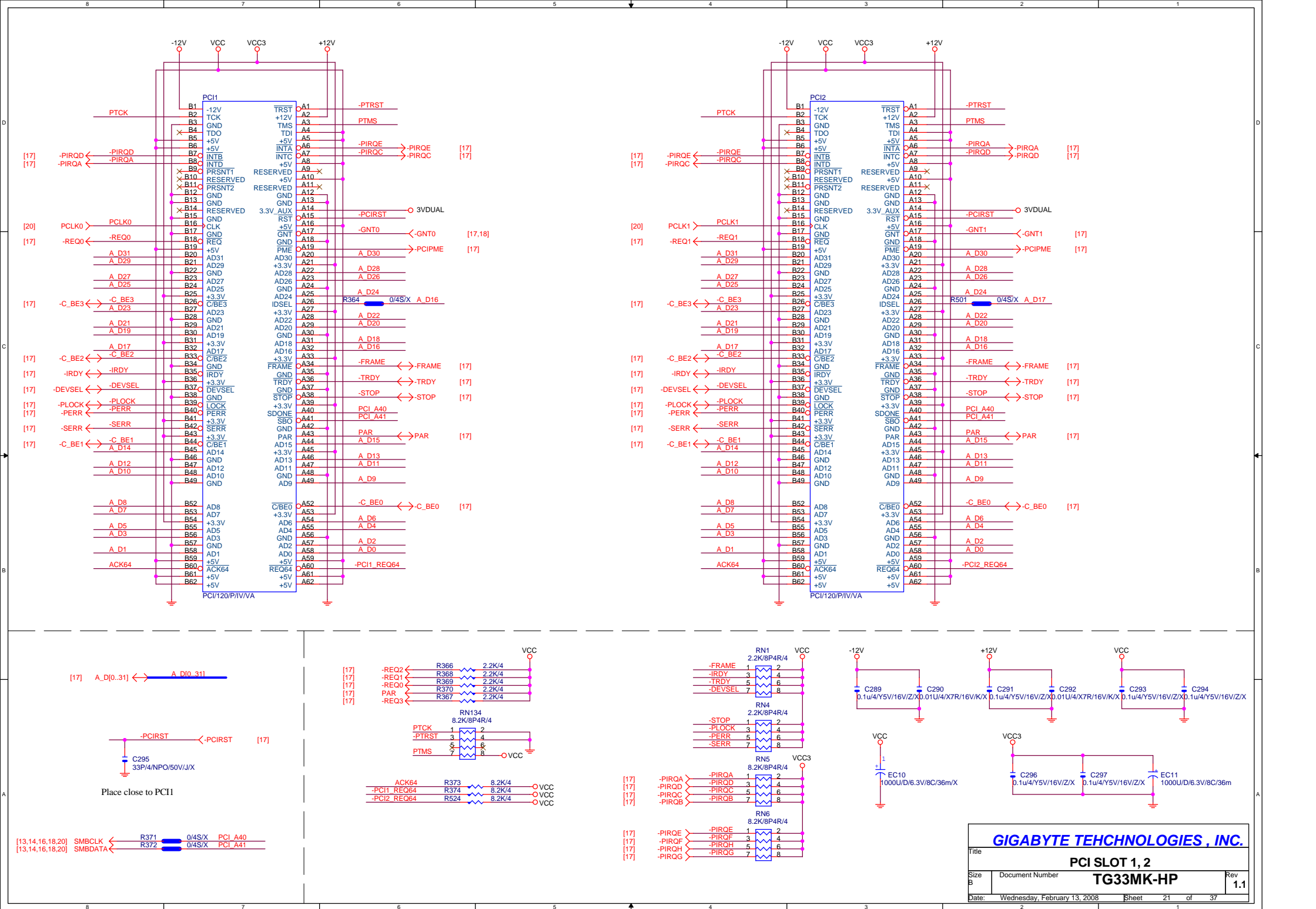
SIGNAL NAME	NO LAN
VccCL_1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	Vcc3_3

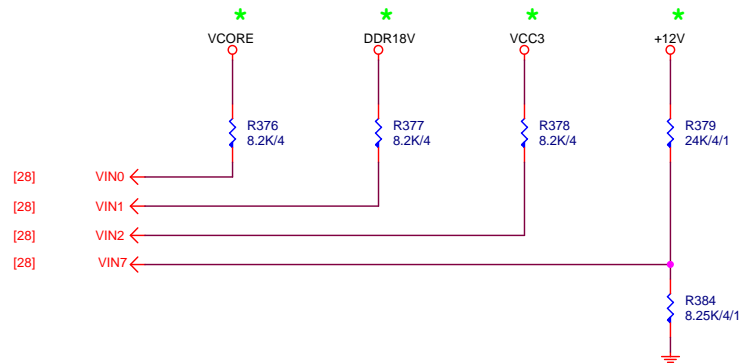
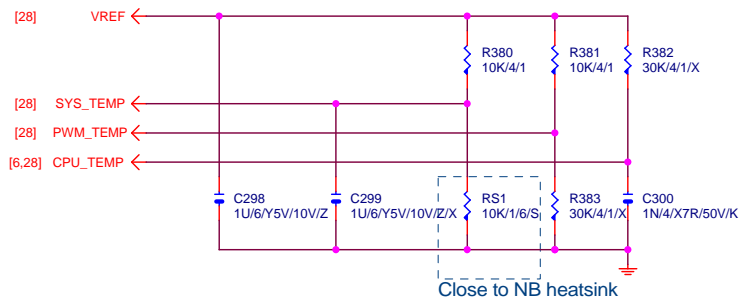
ICH9 Maximum Power Consumption

Power Plane	Maximum Power Consumption			
Symbol	S0	S3 COLD	S4/S5	G3
V5Ref	2mA	NA	NA	NA
V5RefSus	1mA	1mA	1mA	NA
Vcc3_3	308mA	NA	NA	NA
VccSus3_3	212mA	50mA	50mA	NA
VccHDA(3.3V)	32mA	NA	NA	NA
VccSusHDA(3.3V)	32mA	1mA	1mA	NA
VccGLAN3_3	1mA	NA	NA	NA
VccGLAN1_5	80mA	NA	NA	NA
VccLAN3_3	19mA	65mA	65mA	NA
VccLAN1_05	Power by Vcc1_05 in S0	Power by VccLAN3_3 in S3	Power by VccLAN3_3 in S4	NA
VccCL3_3	19mA	71mA	71mA	NA
VccCL1_5	Power by Vcc1_5, A in S0	Power by VccCL3_3 in S3	Power by VccCL3_3 in S4/S5	NA
VccCL1_05	Power by Vcc1_05 in S0	Power by VccCL3_3 in S3	Power by VccCL3_3 in S4/S5	NA
Vcc1_5,A	1.65A	NA	NA	NA
Vcc1_5,B	646mA	NA	NA	NA
VccSus1_5	Power by Vcc1_5, A in S0	Power by VccSus3_3 in S3		
Vcc1_05	1.43A	NA	NA	NA
VccSus1_05	Power by Vcc1_05 in S0	Power by VccSus3_3 in S3	Power by VccLAN3_3 in S4	NA
VccRTC	NA	NA	NA	8uA
VccDMI	41mA	NA	NA	NA
V_CPU_IO	2mA	NA	NA	NA
VccGLANPLL	23mA	NA	NA	NA
VccUSBPLL	11mA	NA	NA	NA

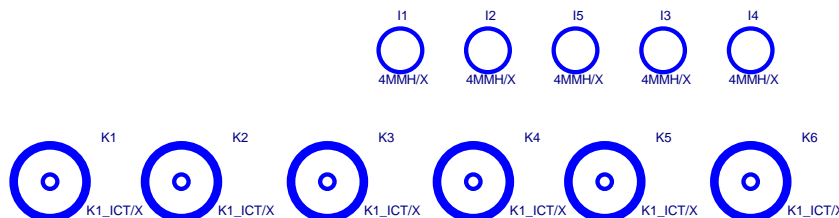
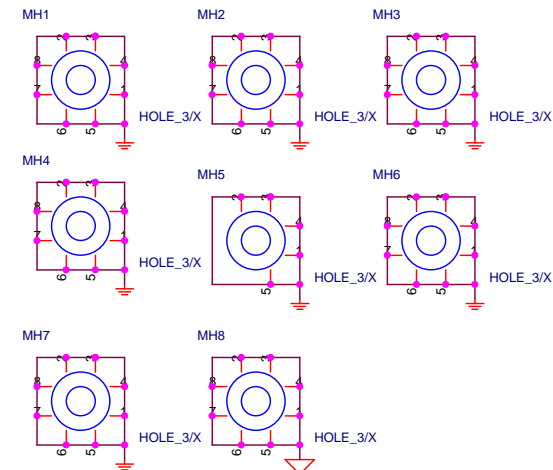
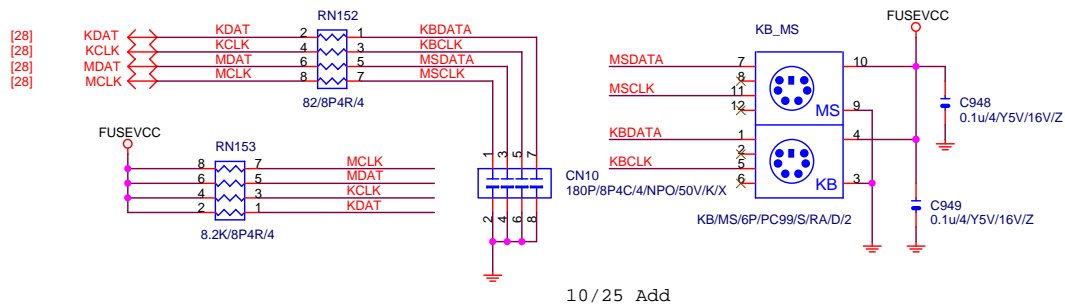
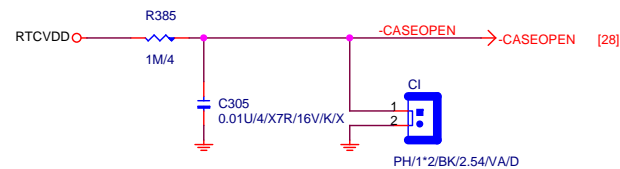
GIGABYTE TECHNOLOGIES, INC.

ICH9-PWR & GND			
File	Document Number	TG33MK-HP	
Size			Rev 1.1
Date	Wednesday, February 13, 2008	Sheet	19 of 37





Case Open Circuits

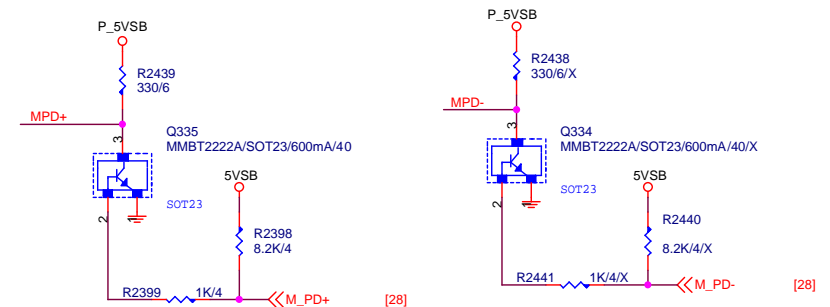
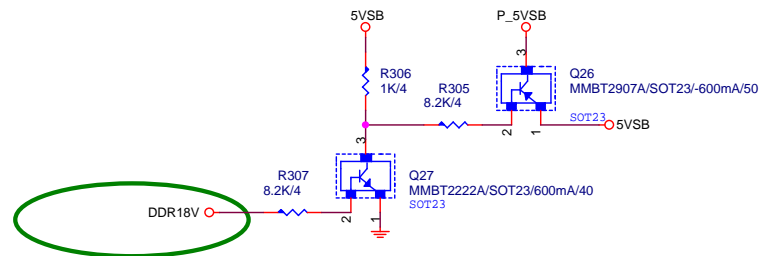
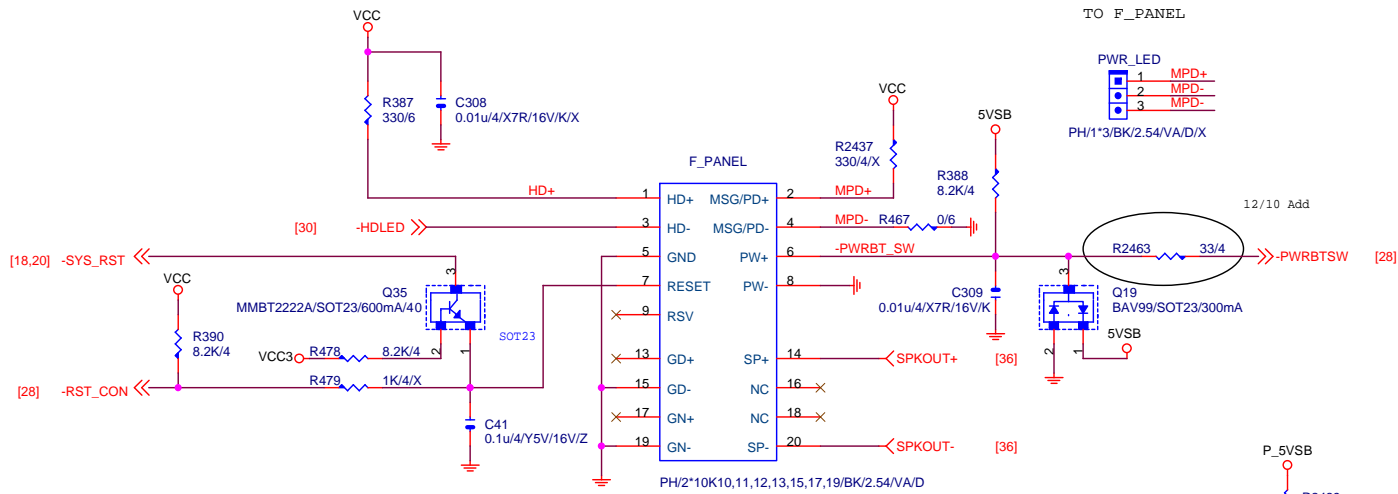


GIGABYTE TECHNOLOGIES, INC.

Title			HARDWARE MONITOR	
Size	Document Number	TG33MK-HP		Rev
B				1.1
Date:	Wednesday, February 13, 2008	Sheet	22	of 37

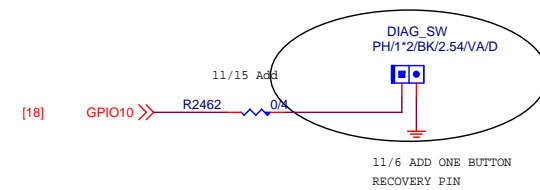
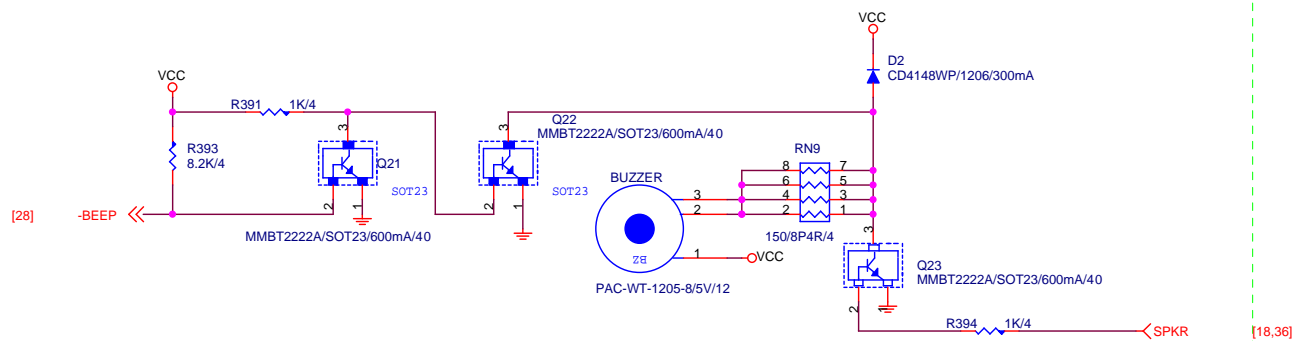
INTEL FRONT PANEL

3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL



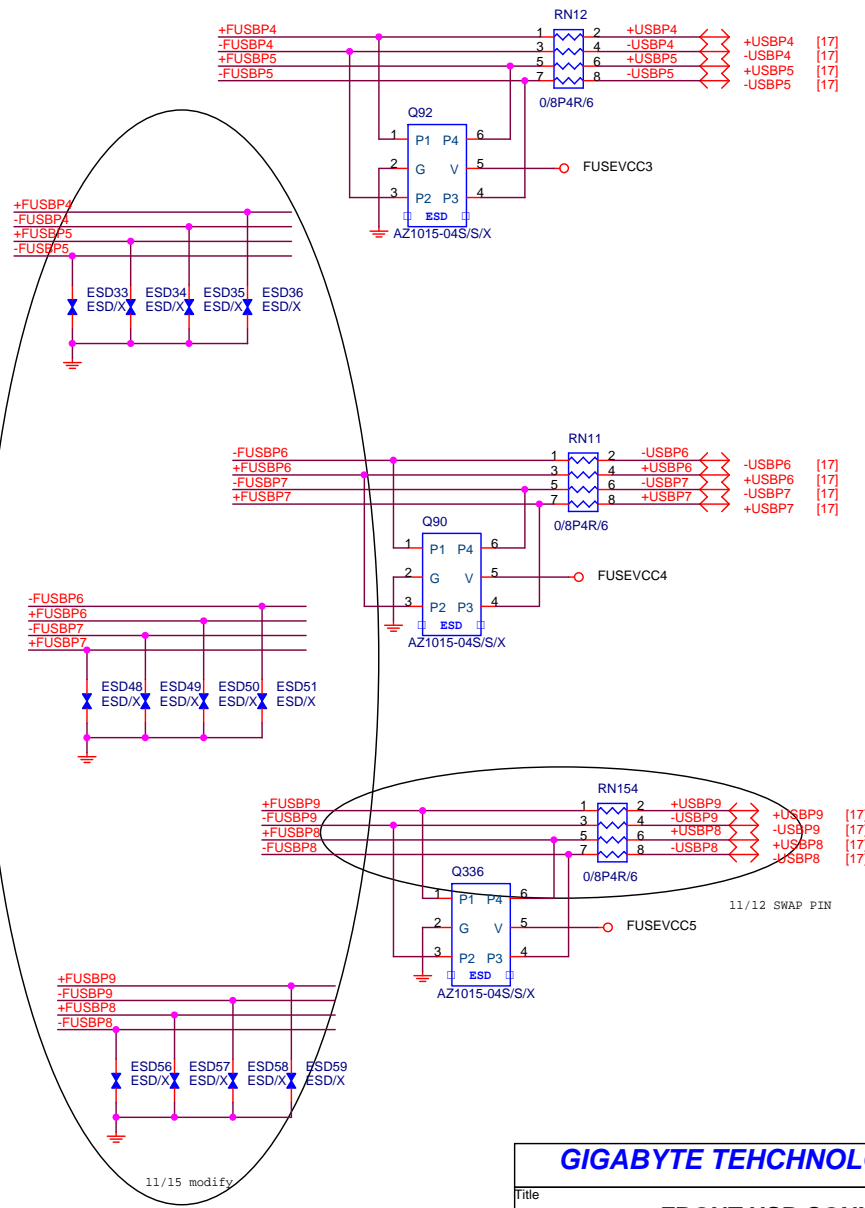
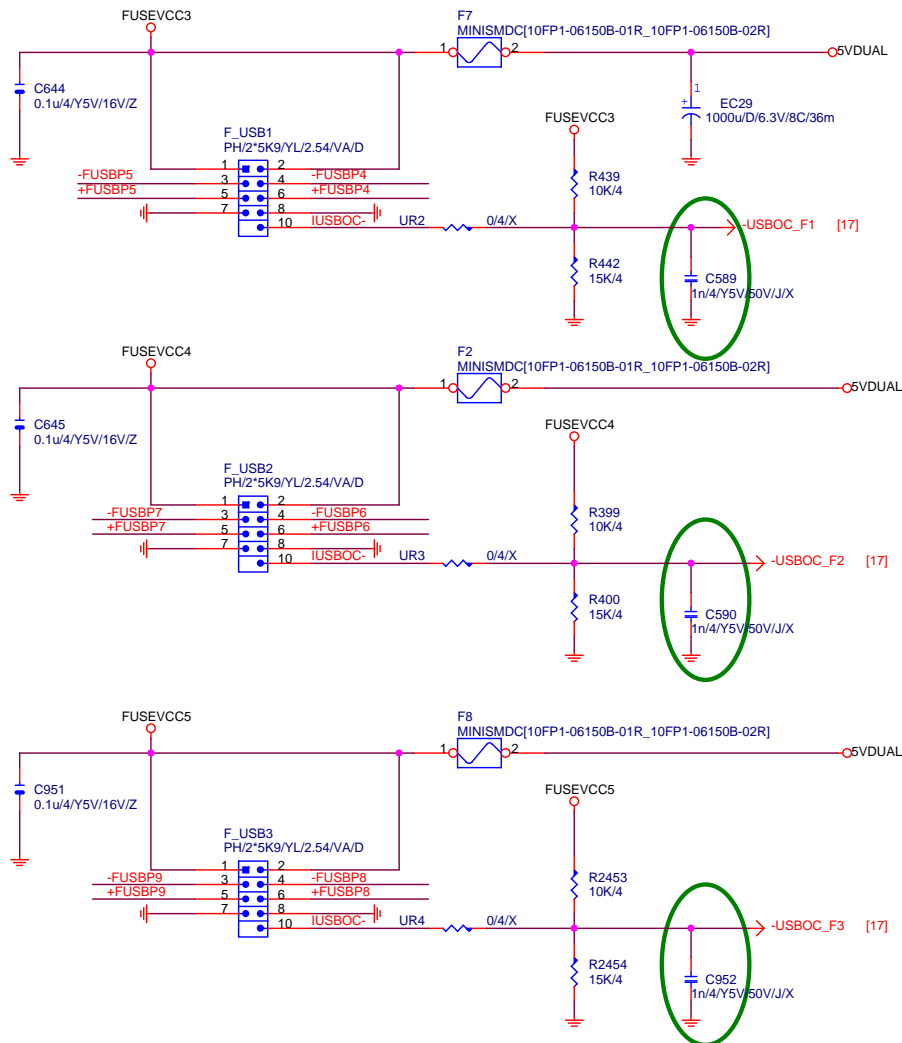
11/6 MODIFY

BUZZER



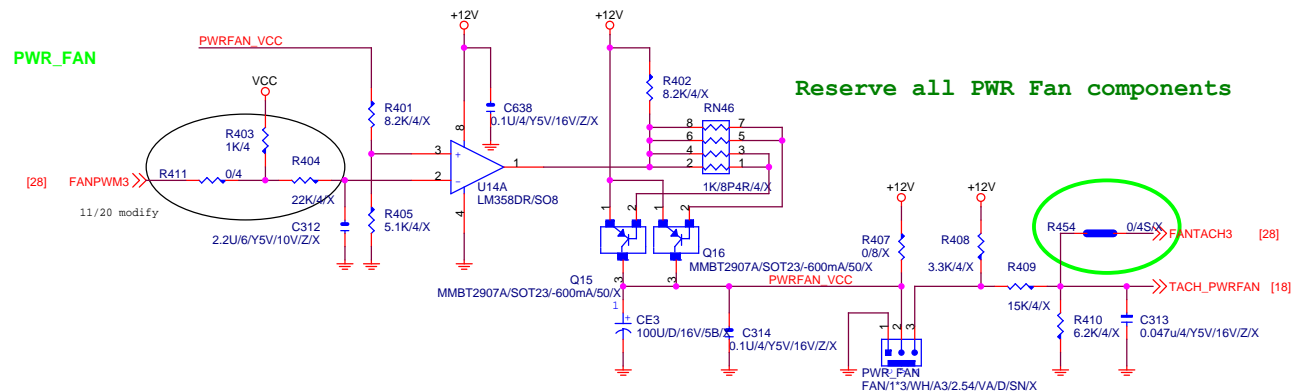
GIGABYTE TECHNOLOGIES, INC.

Title			
FRONT PANEL			
Size B	Document Number	TG33MK-HP	Rev 1.1
Date:	Wednesday, February 13, 2008	Sheet 23 of 37	

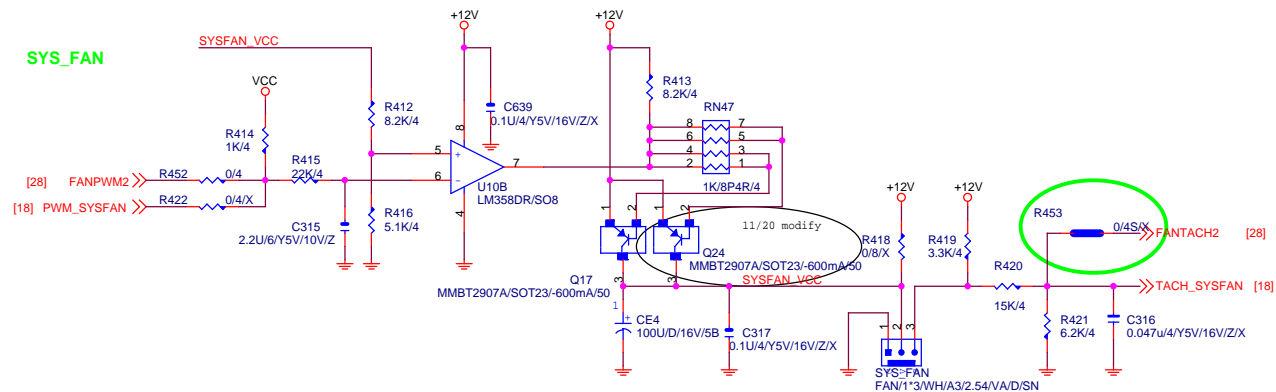


11/15 remove

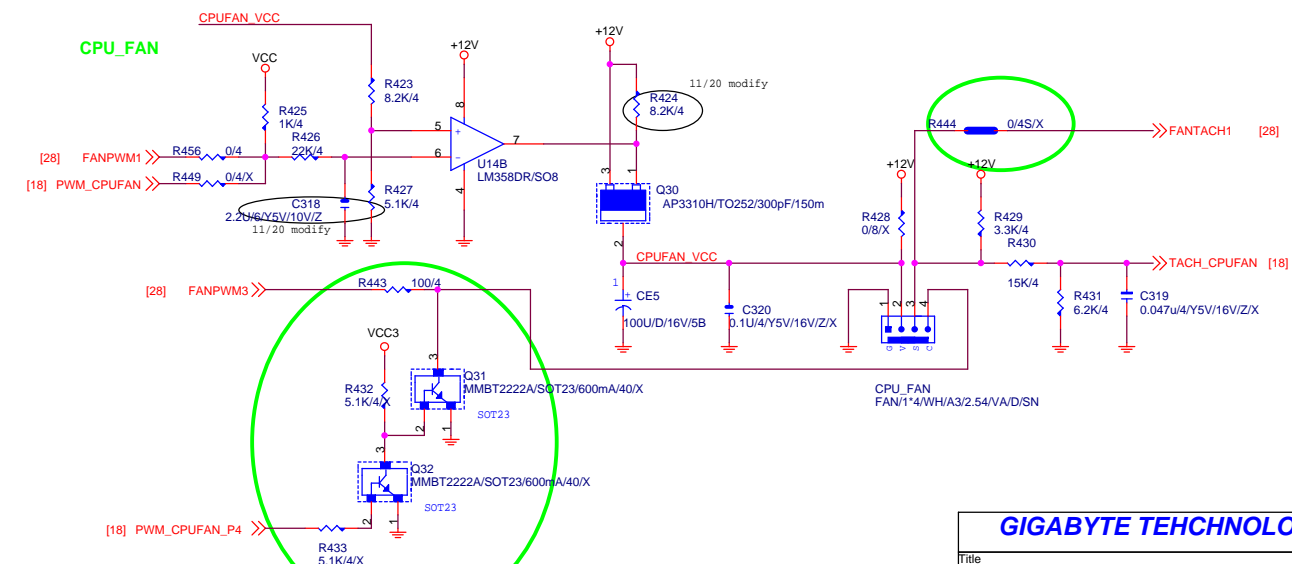
PWR_FAN



SYS_FAN



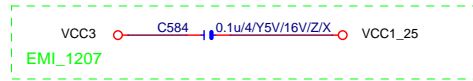
CPU_FAN



GIGABYTE TECHNOLOGIES, INC.

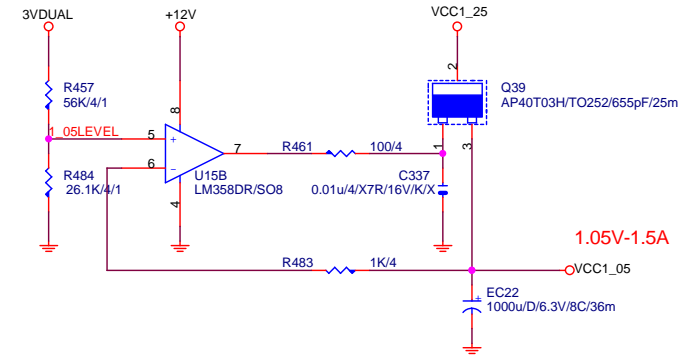
Title			
FAN CONTROL			
Size	Document Number	TG33MK-HP	
Custom			Rev 1.1
Date:	Wednesday, February 13, 2008	Sheet 25	of 37

VCC1_25_CL



REMOVE VCC1_25_CL

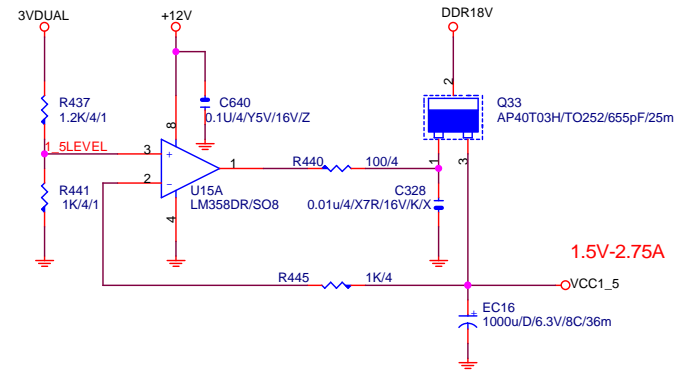
VCC1_05



VCC3_CL

REMOVE VCC3_CL

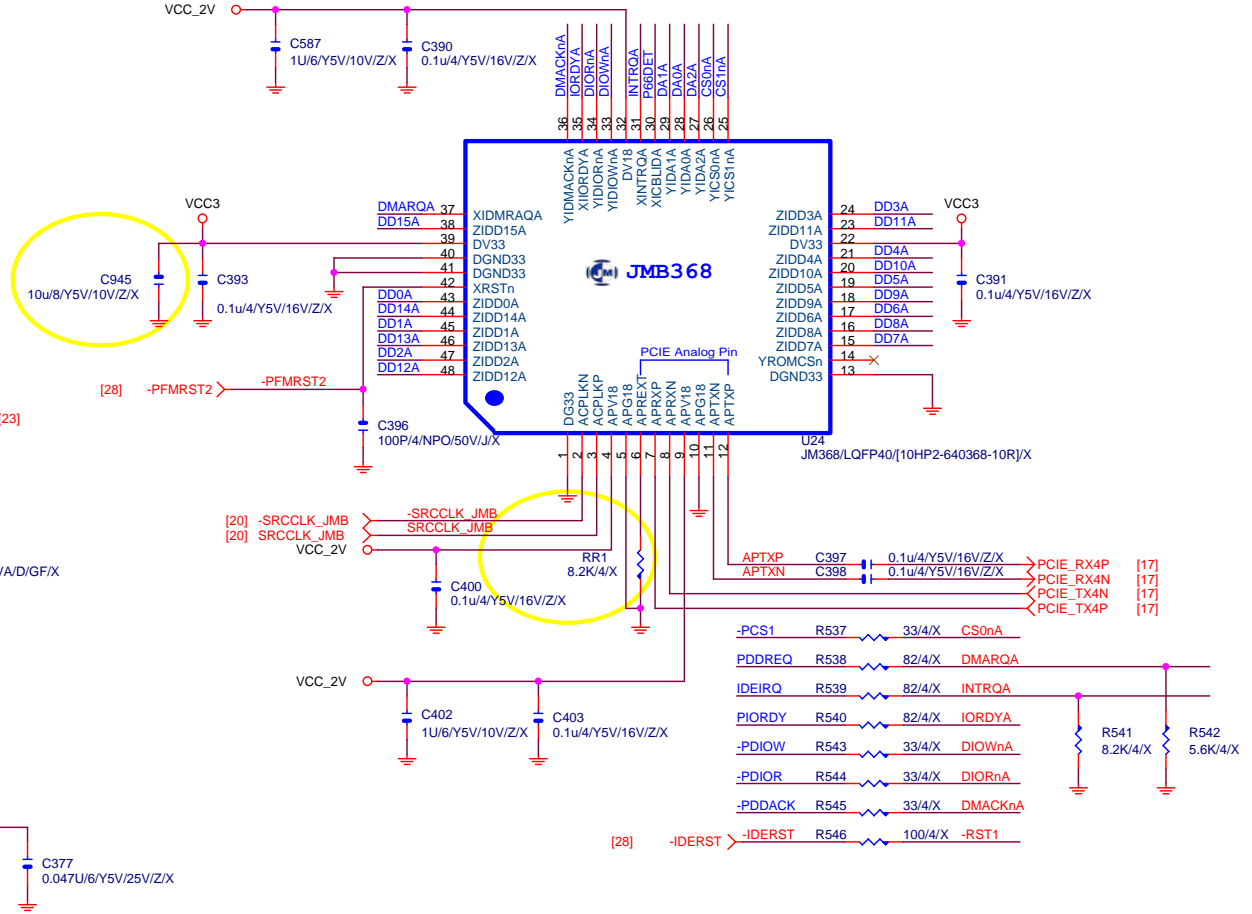
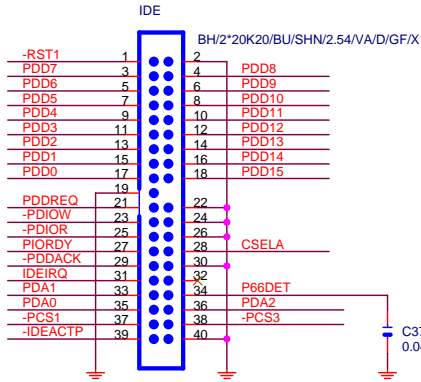
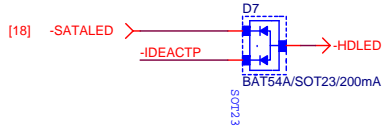
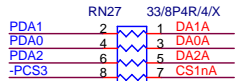
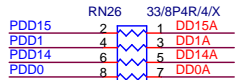
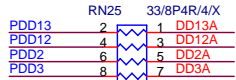
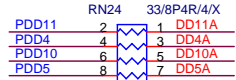
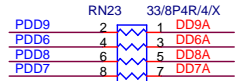
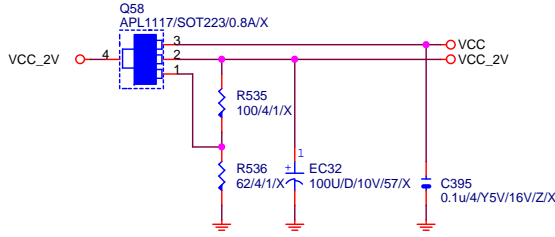
VCC1_5



Title		
<Title>		
Size	Document Number	Rev
B	TG33MK-HP	1.1
Date:	Wednesday, February 13, 2008	Sheet 27 of 37

2.0V VR

$$VCC_2V = 1.25 * (100 + 62 / 100) = 2.0V$$

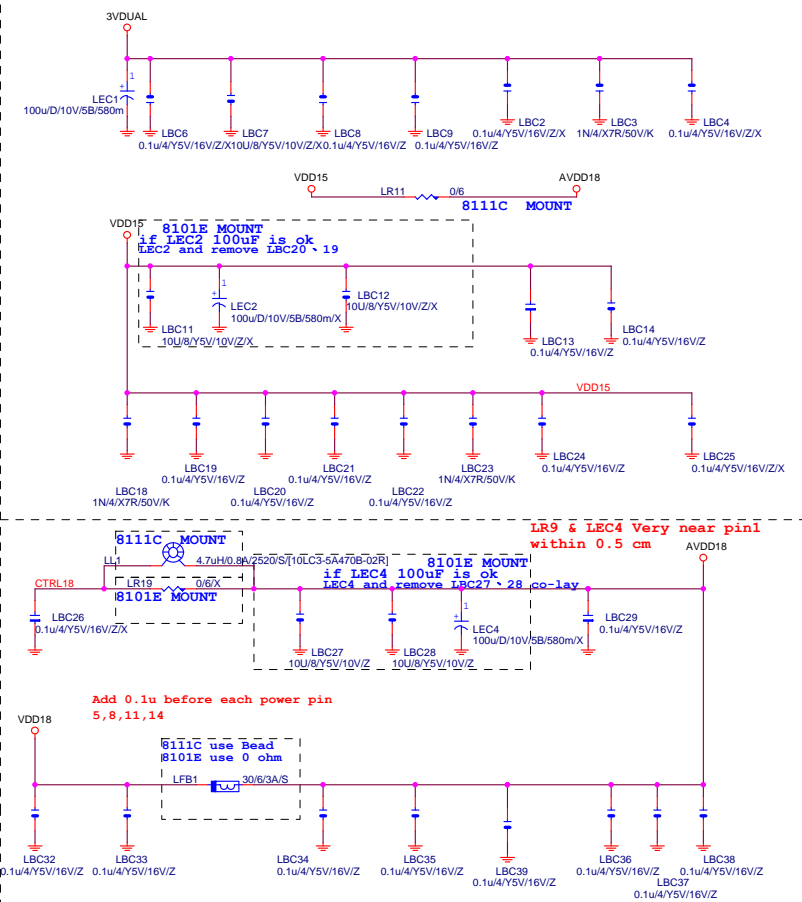
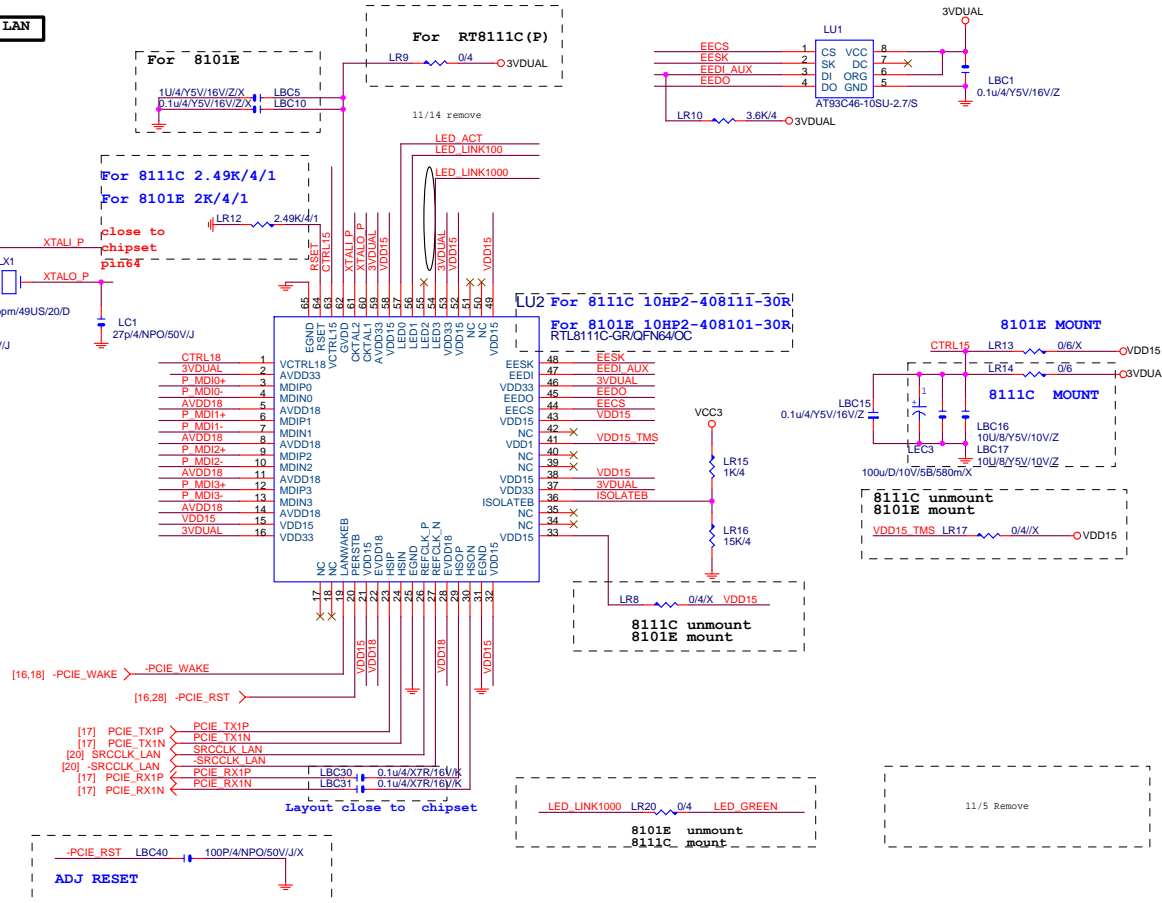


11/7 Default不上

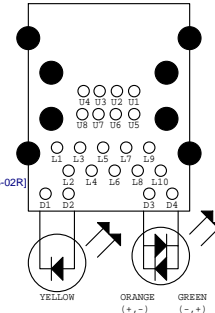
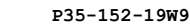
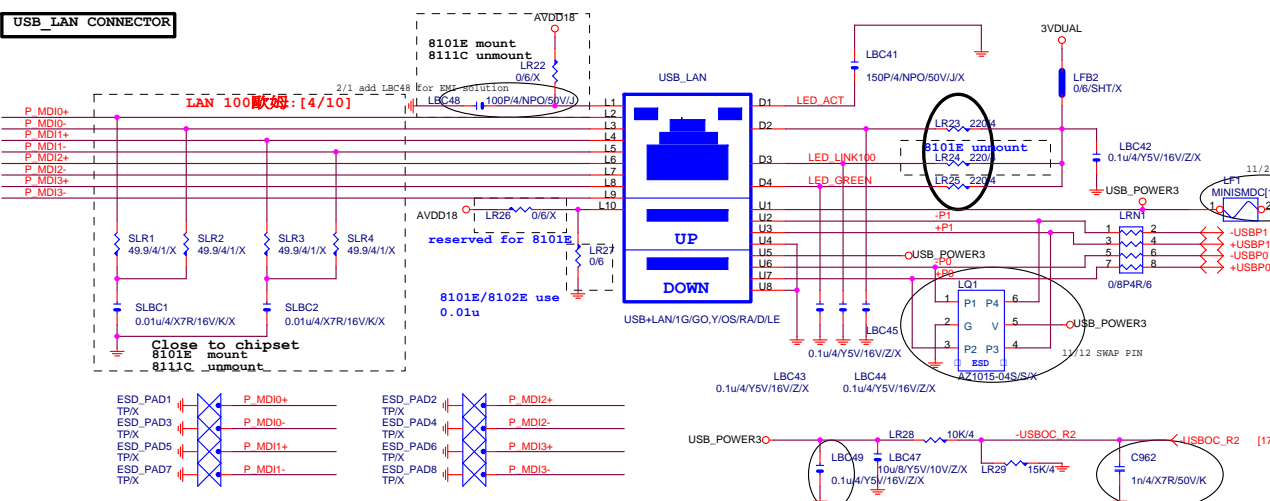
GIGABYTE TECHNOLOGIES, INC.

Title			JMB368 SATA & PATA CONTROLLER
Size			Document Number
B			TG33MK-HP
Date:			Wednesday, February 13, 2008
Sheet			30 of 37
Rev			1.1

PCIE-1G LAN



USB_LAN CONNECTOR




Dual Color LED

D4 D3 Green

D4 D3 Orange

Single Color LED

D2  D1

Yellow


LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/A
LED1	LINK100	LINK10/100/1000	LINK	LINK100/ACT
LED2	LINK10	LINK10/100	Rx	FULL
LED3	LINK1000	LINK1000		LINK1000

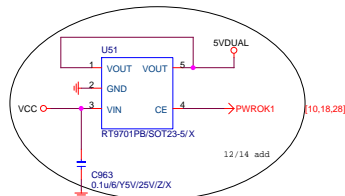
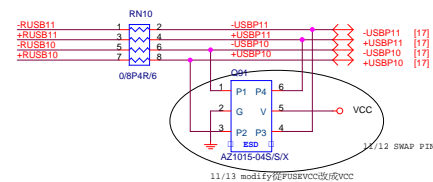
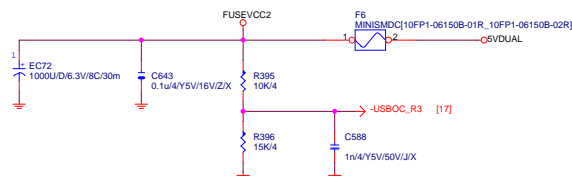
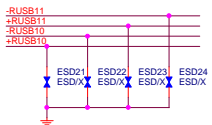
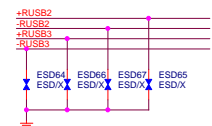
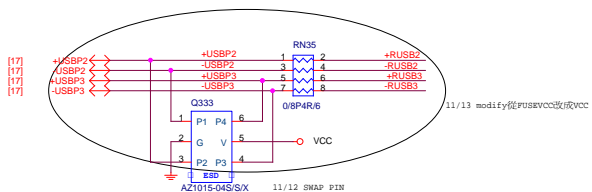
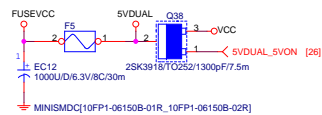
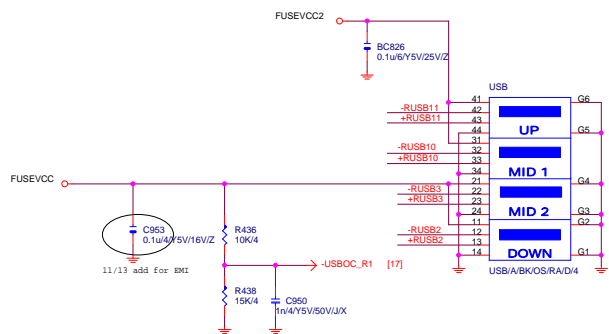
LED3 LINK1000 LINK1000 FULL ACT

*LEDS1-0 Default 11,use 93C46 to change it to 00

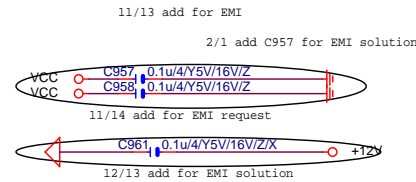
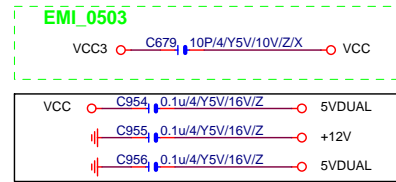
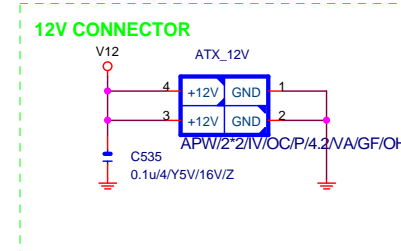
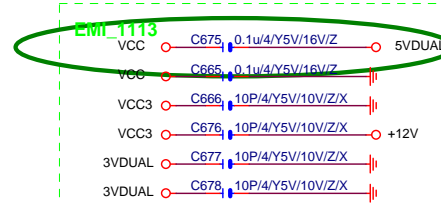
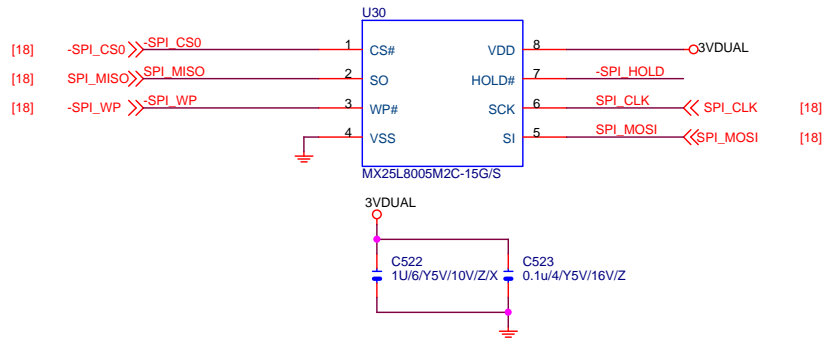
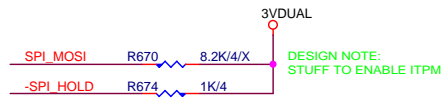
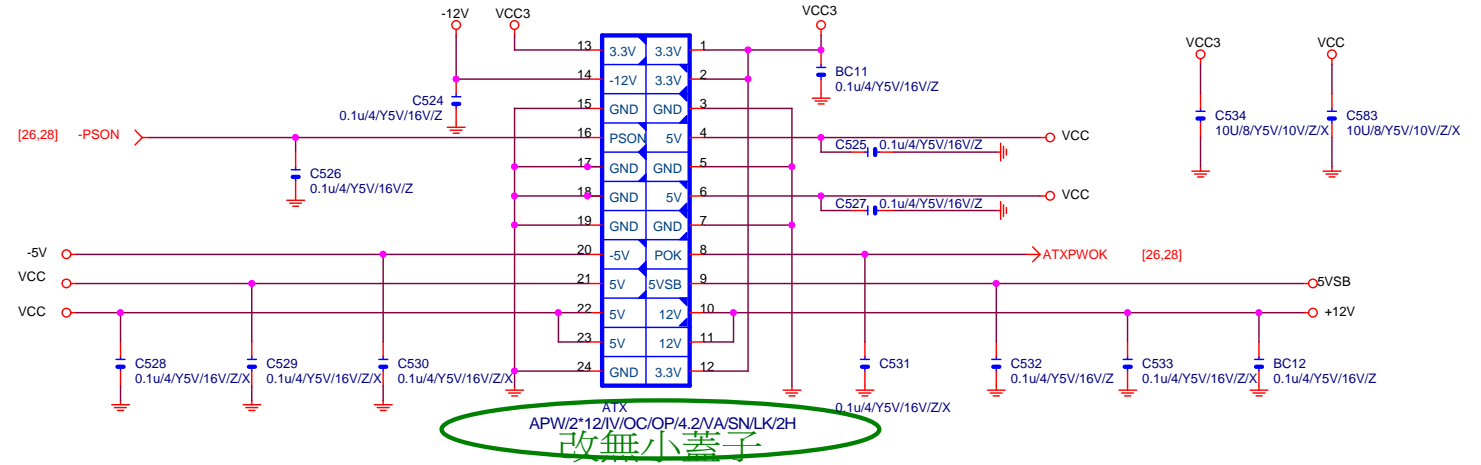
*During power down mode,LED signal are logic high

GIGABYTE TECHNOLOGIES, INC.

Title			
LAN 8111C/ 8101E			
Size	Document Number	Rev	
Custom	<p>  </p> <p> TG33MK-HP </p>	1.1	
Date:	Wednesday, February 13, 2008	Sheet	32 of 37



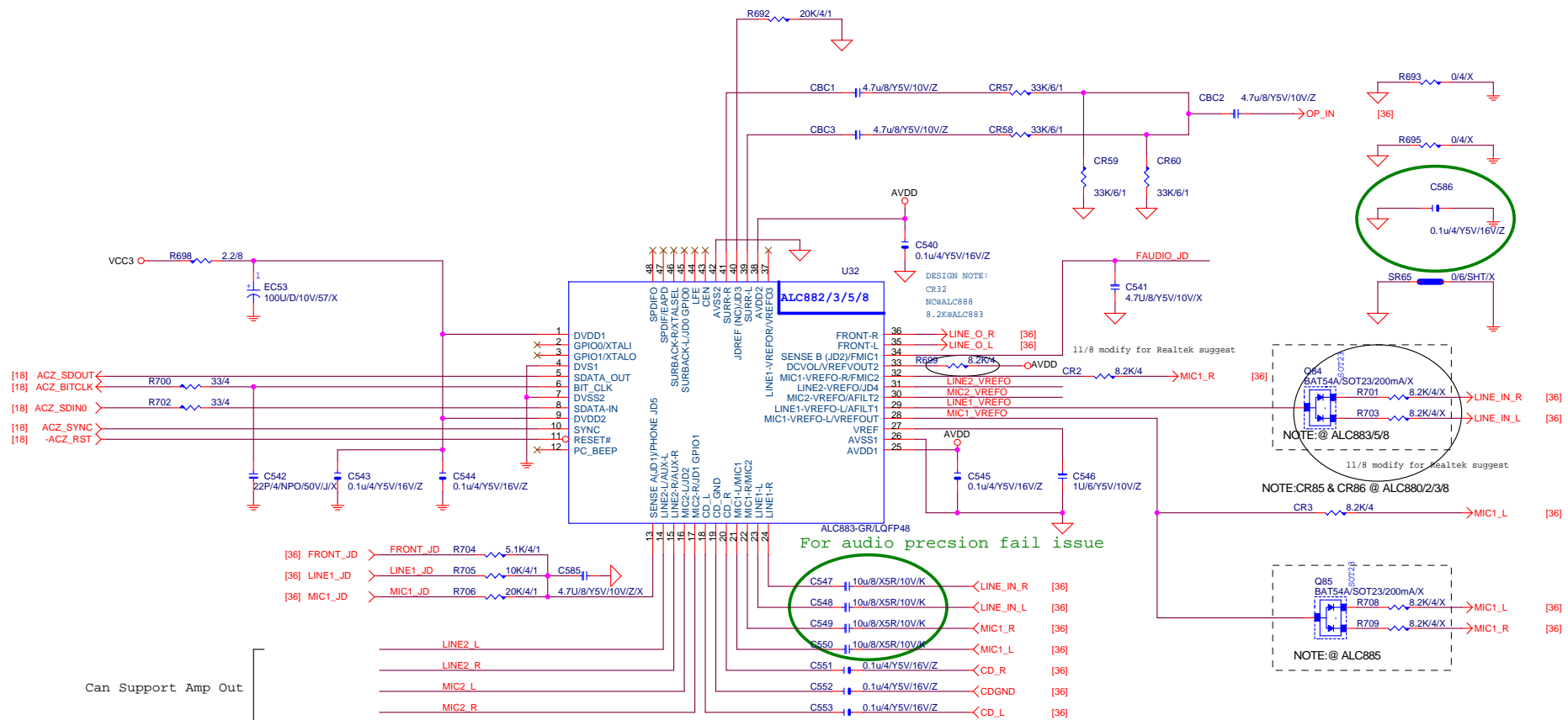
ATX POWER CONNECTOR



GIGABYTE TECHNOLOGIES, INC.

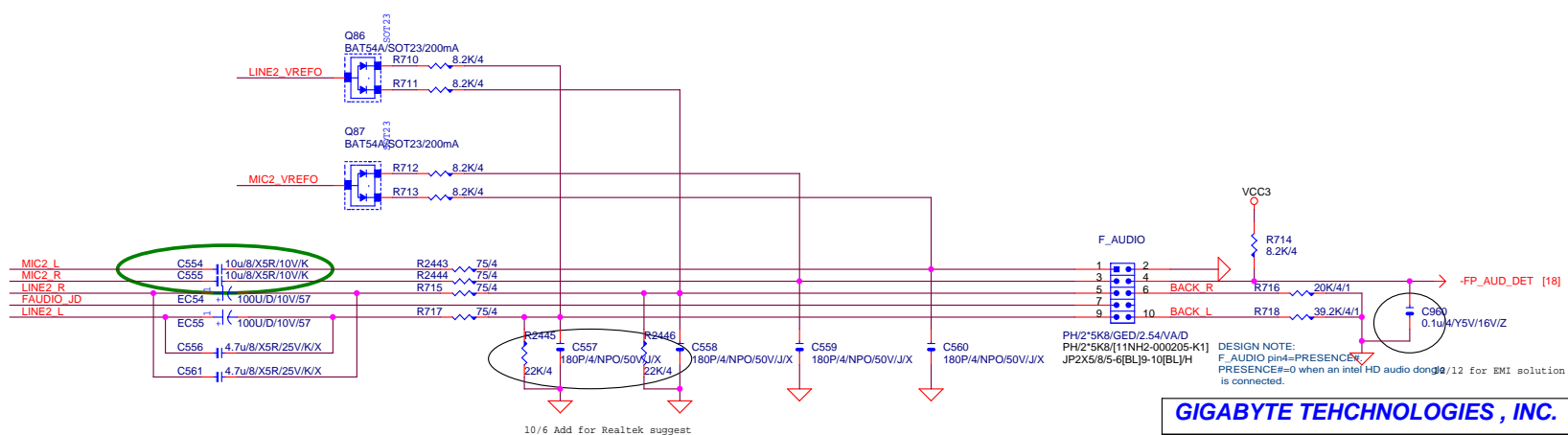
Title			ATX / TPM / OTHERS POWER
Size	Document Number		Rev
B	TG33MK-HP		1.1
Date:	Wednesday, February 13, 2008	Sheet	34 of 37

HD AUDIO CODEC



Can Support Amp Out

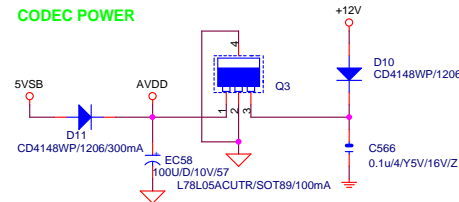
HD AUDIO FRONT PANEL



GIGABYTE TECHNOLOGIES, INC.

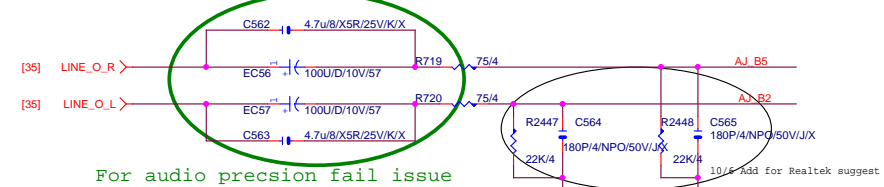
Title			ALC883
Size			Custom
Document Number			TG33MK-HP
Rev			1.1
Date:	Wednesday, February 13, 2008	Sheet	35 of 37

CODEC POWER

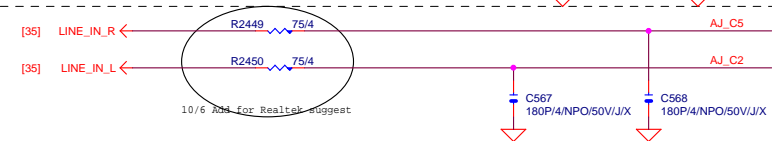


11/13 remove

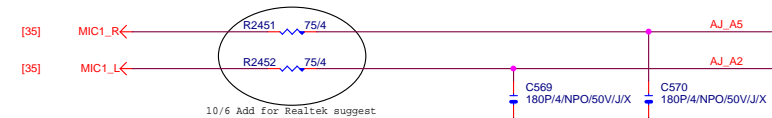
LINE OUT



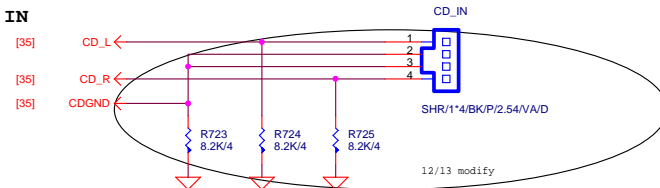
LINE-IN



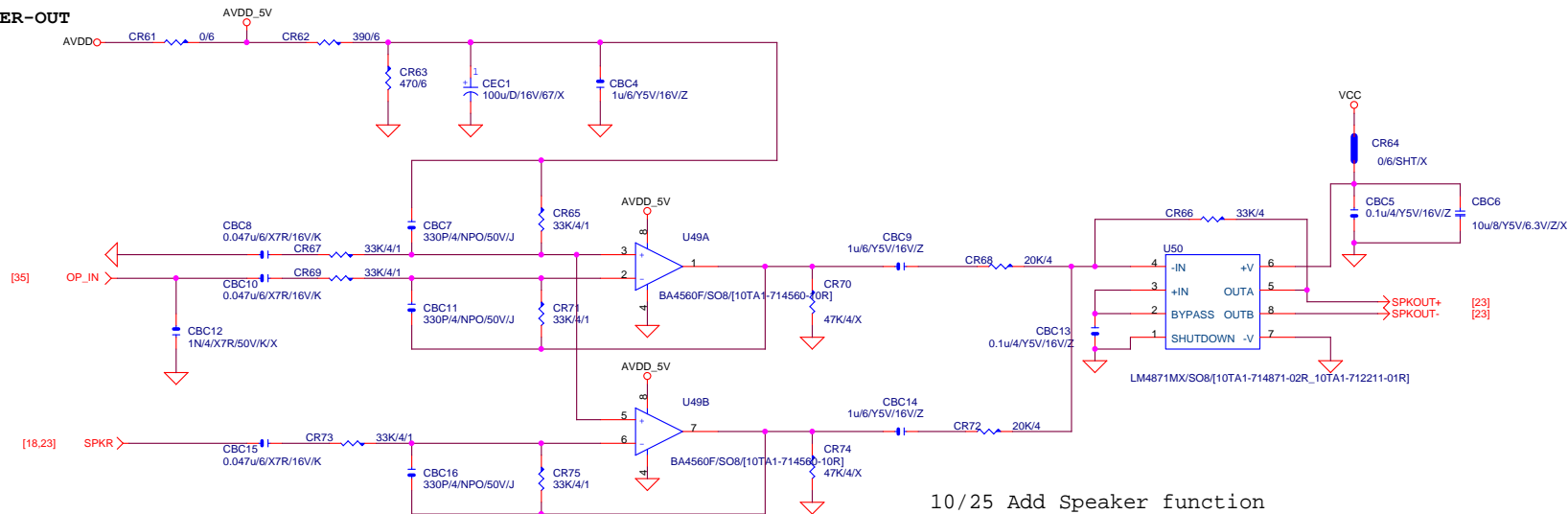
MIC-IN



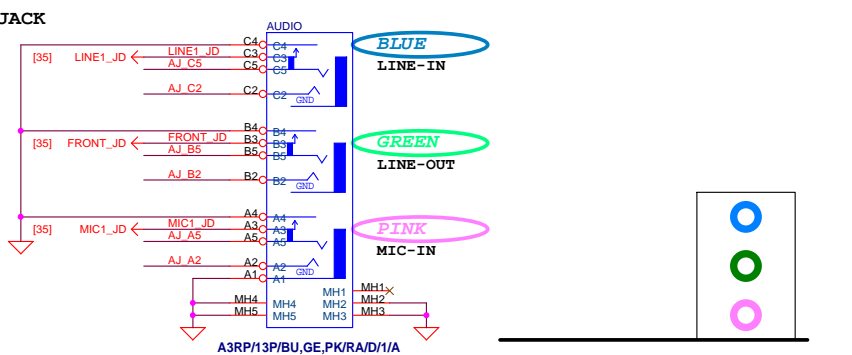
CD IN



SPEAKER-OUT



HDA JACK



GIGABYTE TECHNOLOGIES, INC.

Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	TG33MK-HP	1.1
Date:	Wednesday, February 13, 2008	Sheet 36 of 37

ICH9 GPIO TABLE

GPIO	Signal Name
GPIO_0	-FP_AUD_DET
GPIO_1	TACH_SYSFAN
GPIO_2	-PIRQE
GPIO_3	-PIRQF
GPIO_4	-PIRQG
GPIO_5	-PIRQH
GPIO_6	TACH_PWRFAN
GPIO_7	N/C
GPIO_8	N/C
GPIO_9	N/C
GPIO_10	WOL_ONLY
GPIO_11	-SMBALRT
GPIO_12	LAN_DISABLE
GPIO_13	N/C
GPIO_14	N/C
GPIO_15	-CK_PCI_STOP
GPIO_16	BOARDID0
GPIO_17	TACH_CPUFAN
GPIO_18	BOARDID0
GPIO_19	N/C
GPIO_20	-LPCPME
GPIO_21	N/C
GPIO_22	N/C
GPIO_23	N/C
GPIO_24	GPIO_VSM_AMT_LED
GPIO_25	-CK_CPU_STOP
GPIO_26	N/C
GPIO_27	N/C
GPIO_28	N/C
GPIO_29	-USBOC_F1
GPIO_30	-USBOC_F2
GPIO_31	-USBOC_F2
GPIO_32	-PWRLED_CTRL
GPIO_33	-GD_CTRL
GPIO_34	-SLP_BTN
GPIO_35	N/C
GPIO_36	N/C
GPIO_37	N/C
GPIO_38	N/C
GPIO_39	N/C
GPIO_40	-USBOC_R1
GPIO_41	-USBOC_R2
GPIO_42	-USBOC_R2
GPIO_43	-USBOC_F1
GPIO_44	-USBOC_F3
GPIO_45	-USBOC_F3

IT8718 GPIO TABLE

GPIO	Signal Name
GPIO_46	N/C
GPIO_47	N/C
GPIO_48	N/C
GPIO_49	N/C
GPIO_50	-REQ1
GPIO_51	N/C
GPIO_52	-REQ2
GPIO_53	N/C
GPIO_54	-REQ3
GPIO_55	-GNT3
GPIO_56	1_WATT_CTRL_1
GPIO_57	-SPI_WP
GPIO_58	N/C
GPIO_59	-USBOC_R1
GPIO_60	-LINKALERT

GPIO	Signal Name
GPIO_10	-FP_AUD_DET
GPIO_11	TACH_SYSFAN
GPIO_12	-PIRQE
GPIO_13	-PIRQF
GPIO_14	-PIRQG
GPIO_17	-PIRQH
GPIO_21	TACH_PWRFAN
GPIO_23	N/C
GPIO_24	N/C
GPIO_25	N/C
GPIO_10	WOL_ONLY
GPIO_11	-SMBALRT
GPIO_12	LAN_DISABLE
GPIO_13	N/C
GPIO_14	N/C
GPIO_15	-CK_PCI_STOP
GPIO_16	BOARDID0
GPIO_17	TACH_CPUFAN
GPIO_18	BOARDID0
GPIO_19	N/C
GPIO_20	-LPCPME
GPIO_21	N/C
GPIO_22	N/C
GPIO_23	N/C
GPIO_24	GPIO_VSM_AMT_LED
GPIO_25	-CK_CPU_STOP
GPIO_26	N/C
GPIO_27	N/C
GPIO_28	N/C
GPIO_29	-USBOC_F1
GPIO_30	-USBOC_F2
GPIO_31	-USBOC_F2
GPIO_32	-PWRLED_CTRL
GPIO_33	-GD_CTRL
GPIO_34	-SLP_BTN
GPIO_35	N/C
GPIO_36	N/C
GPIO_37	N/C
GPIO_38	N/C
GPIO_39	N/C
GPIO_40	-USBOC_R1
GPIO_41	-USBOC_R2
GPIO_42	-USBOC_R2
GPIO_43	-USBOC_F1
GPIO_44	-USBOC_F3
GPIO_45	-USBOC_F3

PWROK/RESET Table:

ITE8716KX	NET NAME	TARGET
PIN62/PCIRST1#(O)	-EXT_RST	TPM, EXT_DUAL_BIOS
PIN64/PCIRST2#(O)	-BIOSRST	LPC ROM
PIN65/PCIRST3#(O)	NC	NC
PIN115/PCIRST4#(O)	-THRMO	MCP51
PIN68/LRESET#(I)	-LPCRST	ITE8716KX
PIN63/PWROK	PWOK1	FRONT USB PWR(VCC) CONTROL
PIN109/PWROK2	PWOK2	1. THERM SHUTDOWN CIRCUIT 2. PWRGD DELAY 3. REAR USB PWR(VCC) CONTROL